Thunderbolt over Type-C
Overcoming Test Challenges

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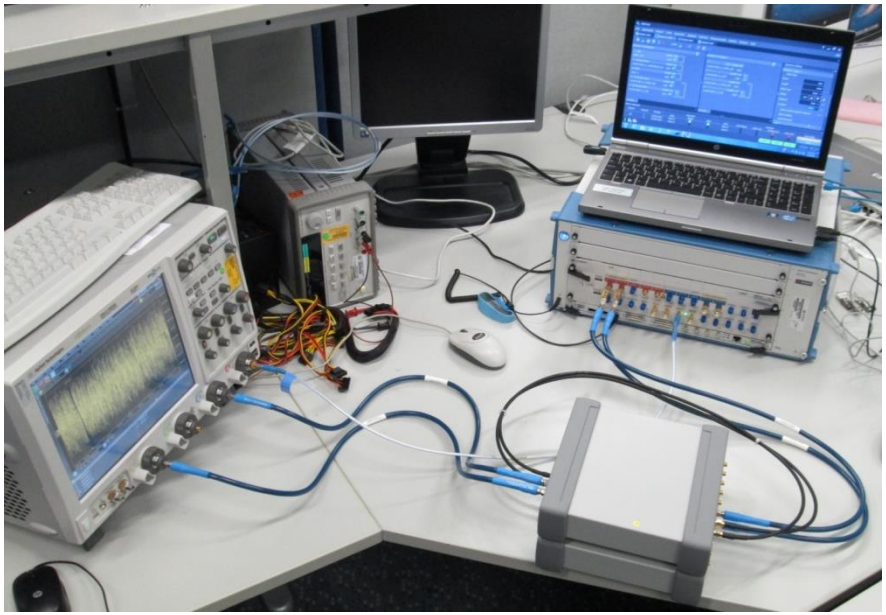


KEYSIGHT TECHNOLOGIES

Agenda

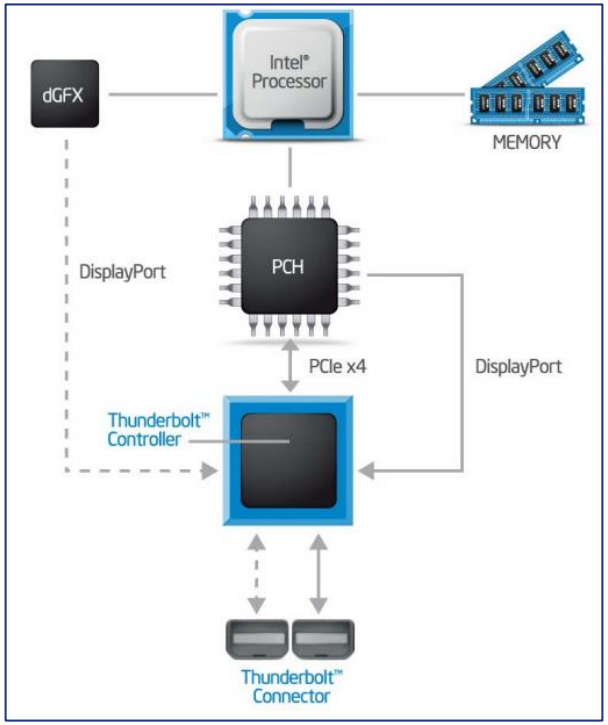
- Thunderbolt 3 Overview
- Measurement Challenges
- Tx Testing Solution
- Return Loss Testing
- Power Delivery Testing
- Rx Testing Solution
- Summary

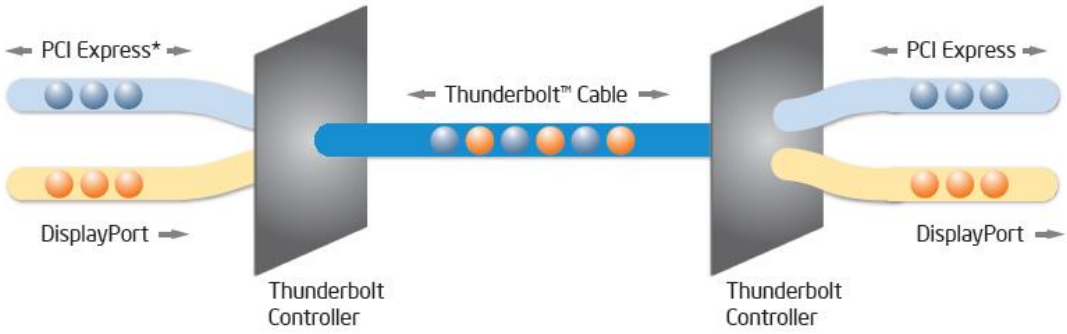
What is Thunderbolt?

– Thunderbolt features two bidirectional (full duplex) channels that run up to 20Gbps each and allows daisy-chaining of up to six devices.

– Passive or active Cable

– Thunderbolt tunnels two protocols (PCI Express and DisplayPort) when running in native Thunderbolt mode.

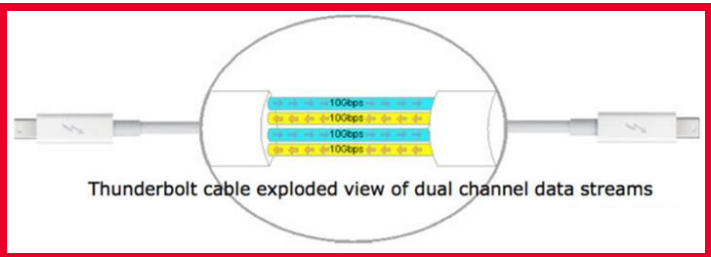




Evolution of Thunderbolt

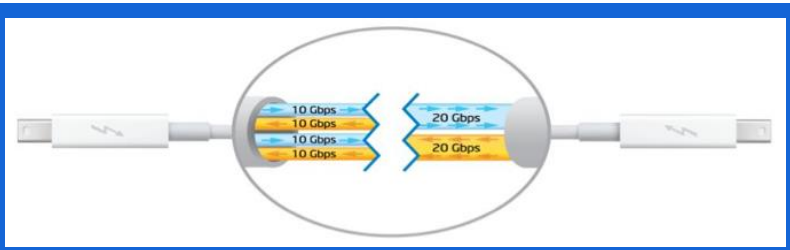
Thunderbolt 1

4-lane 10 Gbps	2ch 10Gbps	2011



Thunderbolt 2

4-lane 10 Gbps	1ch 20Gbps	2013

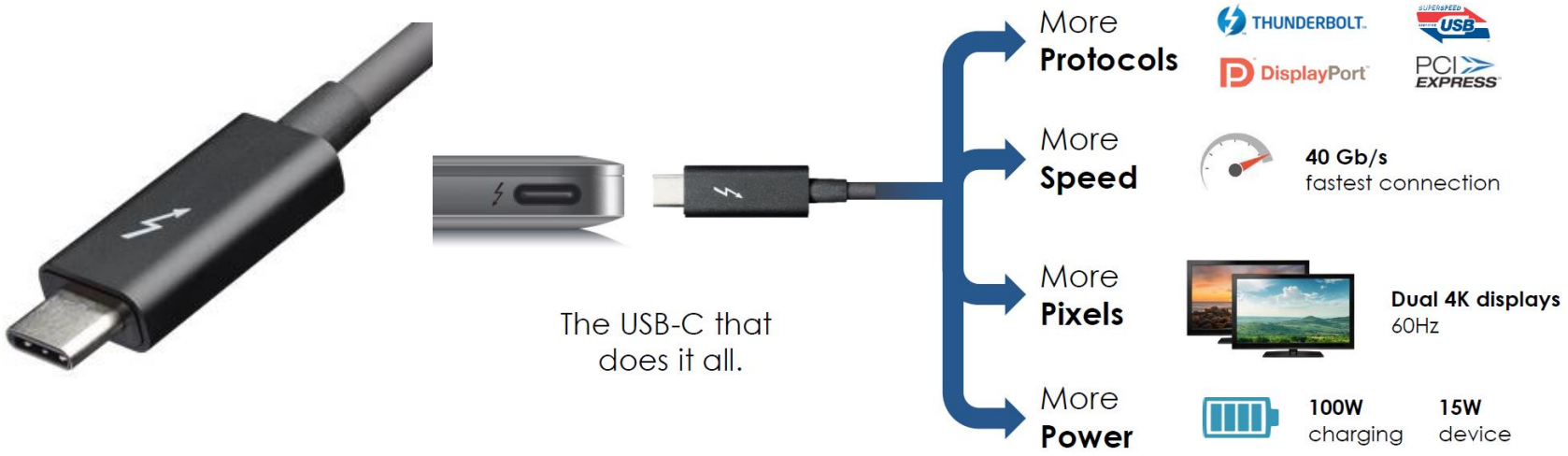


Thunderbolt 3

4-lane 20 Gbps	1ch 40Gbps	2015

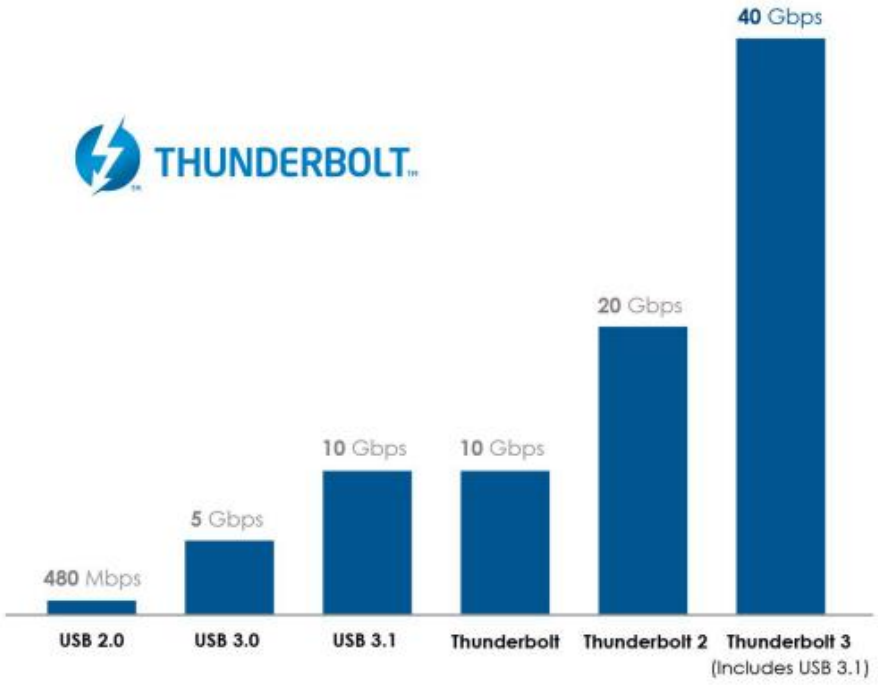
Thunderbolt 3 Overview

- Announced in Q2 2015
- Uses the Type-C connector
- Channel aggregation: two independent 20Gbps links into one logical 40Gbps link
- Supports other standards through ALT mode
- Cost competitive vs multi-chip, discrete, mux solutions



More Speed

– 40Gb/s Thunderbolt™ 3
  - Bi-directional, PCI Express and DisplayPort
  - Four lanes of PCI Express Gen 3
  - Eight lanes of DisplayPort 1.2
– Native USB 3.1 (up to 10Gb/s)
– Native DisplayPort 1.2



More Possibilities

4K Video

Single-cable docking
with charging

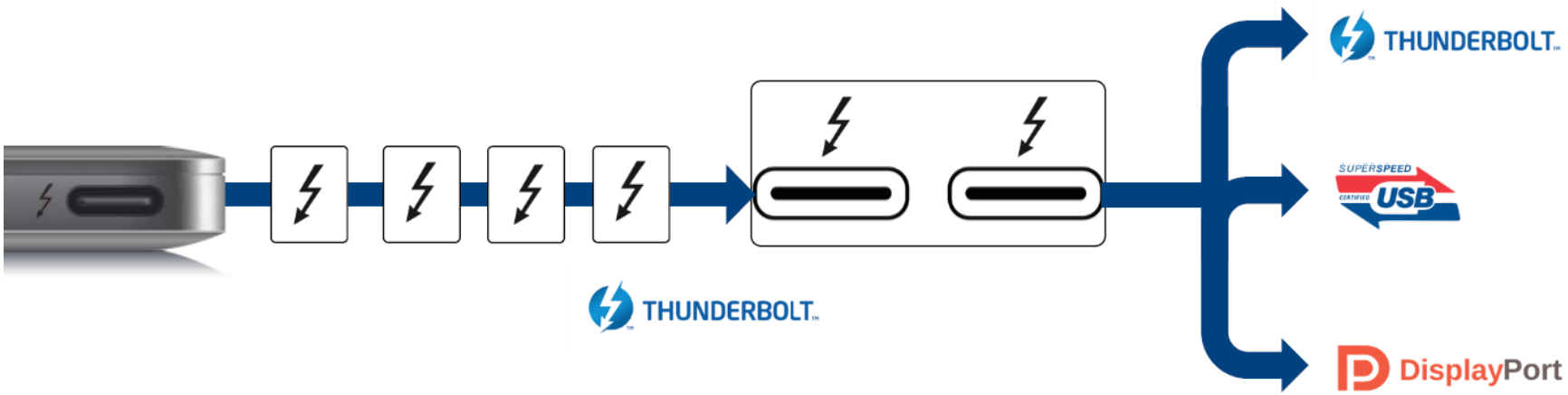
External graphics

Thunderbolt™ networking

Configurations

– Daisy-chain up to six devices if the link is in Thunderbolt mode

– Second device port operates the same as computer port and supports Thunderbolt, USB, and DisplayPort devices



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- Return Loss Testing
- Rx Testing Solution
- Power Delivery Testing
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Testing Methodology

– PHY testing approach will be similar to Thunderbolt 2
  - Tx, Rx, and Return Loss
  - PD for Type-C Alternate Mode
  - DP, USB for Type-C

– Keysight can help with pre-compliance testing

Thunderbolt™ Interconnect Specification

USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification

USB Type-C Thunderbolt Alternate Mode

Measurement Challenges

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How do I ensure the transmitter is in spec?

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Is my receiver capable to dectect signal reliably at 40Gb/s?

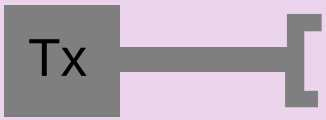
Measurement Challenges

How do I ensure the transmitter is in spec?

Do I need to purchase Test Equipment for Thunderbolt, USB and DisplayPort?

Is my receiver capable to dectect signal reliably at 40Gb/s?

Type-C Design and Test Challenges: Overview



Transmitter Test

USB 3.1
USB 2.0
Alternate modes

Power Delivery

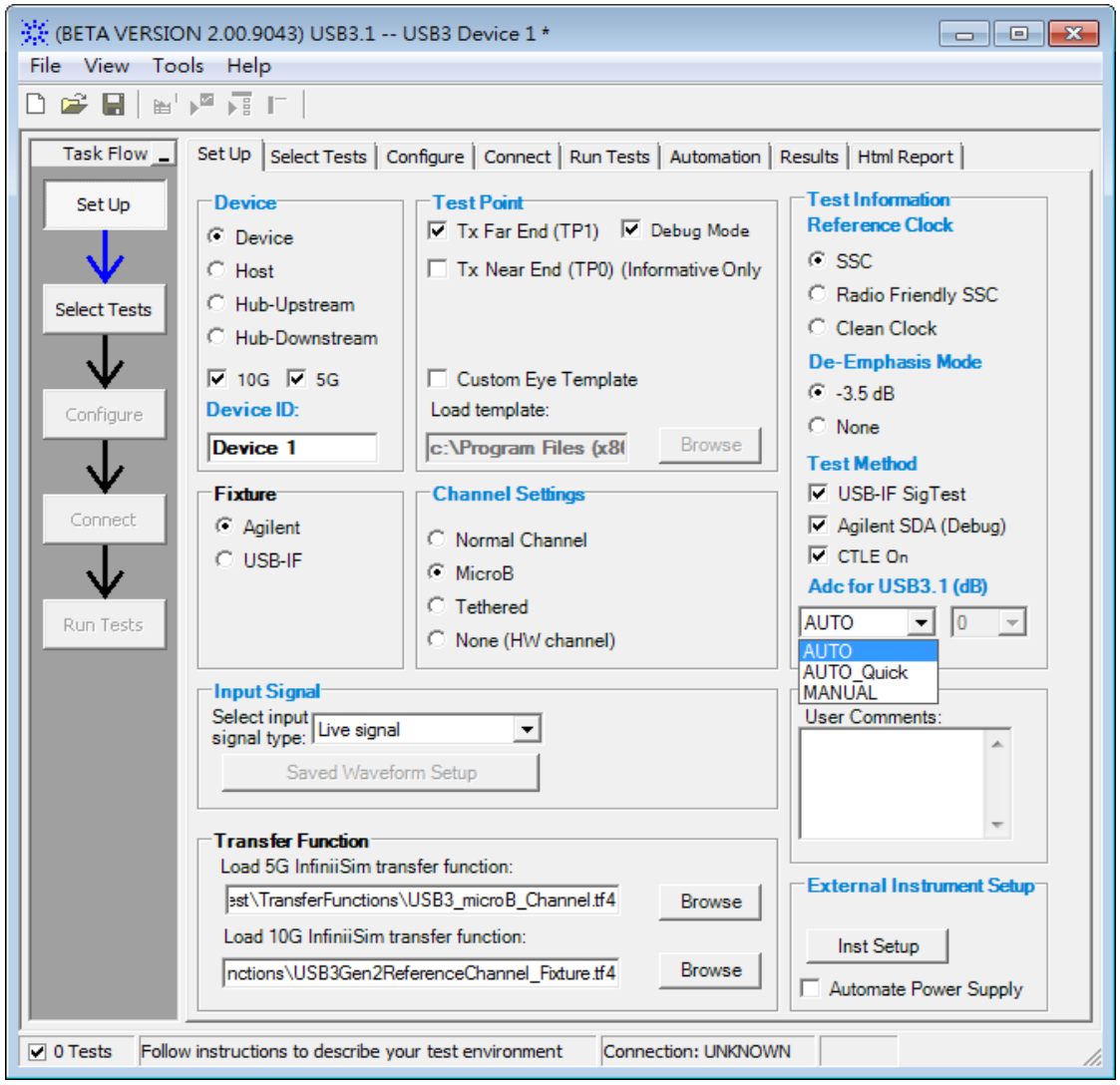
Interconnect Test

Receiver Test

USB 3.1
USB 2.0
Alternate modes

Power Delivery

USB 3.1 TX Compliance Application

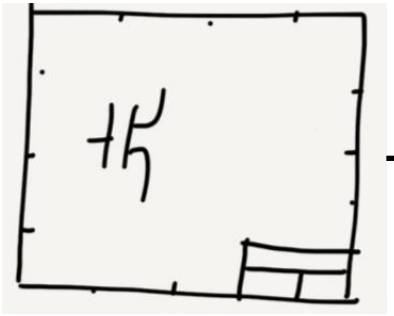


Keysight solution features:

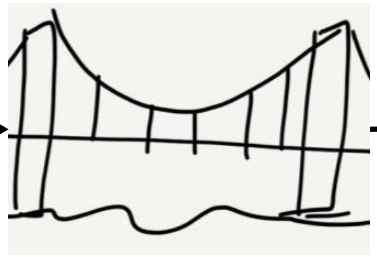
- ✓ Support USB3.1 Gen1/Gen2
- ✓ USB-IF Sigtest & Keysight SDA algorithm
- ✓ CTLE Adc scan
- ✓ Support live & saved waveforms
- ✓ USB-IF and customer's embedded transfer function
- ✓ External instrument for triggering SCD1/2, LBPM and toggle Compliance Pattern

Simulation-Measurement Correlation Challenge

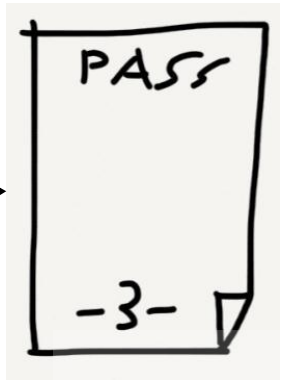
Simulation…



Design and simulate



Bridging script generates report



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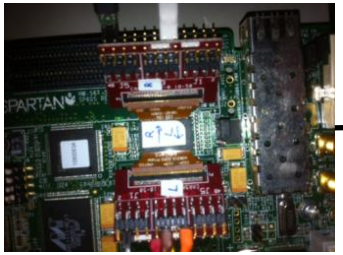
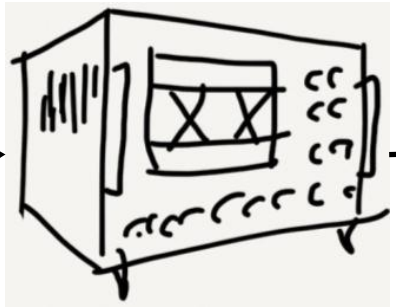
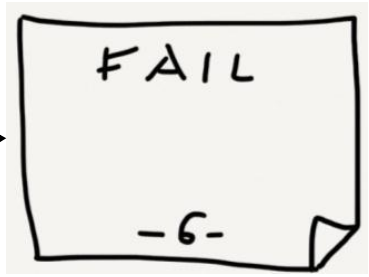
Physical Measurements…



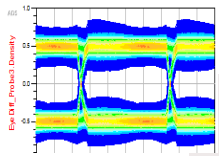
Prototype in lab

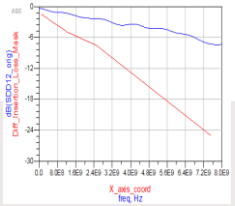


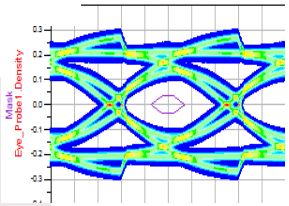
Scope compliance application

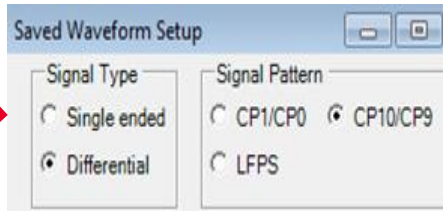


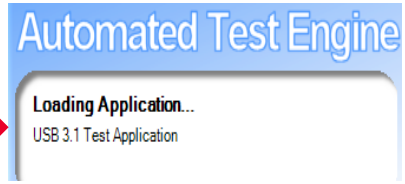
Simulation Test Solutions: Advanced Design System





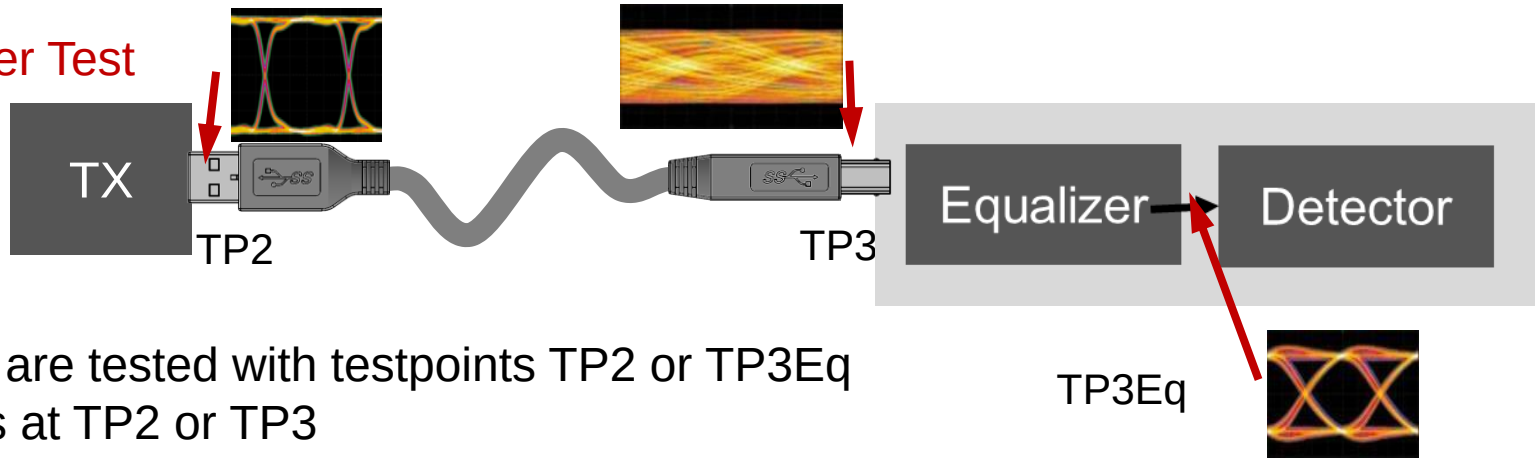






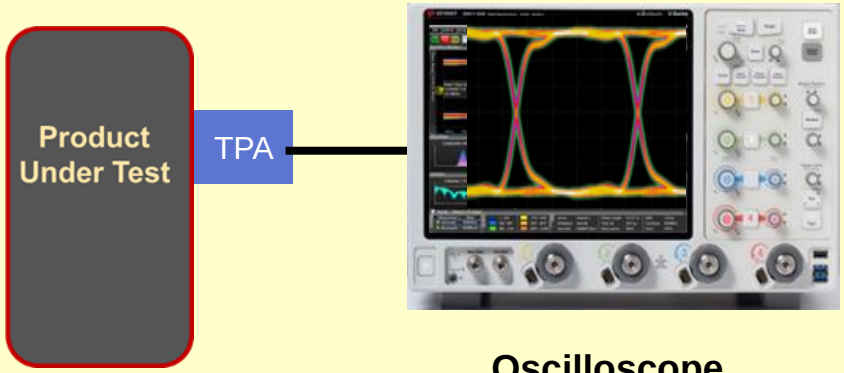
Physical Layer Testing: High speed data lanes

Transmitter Test

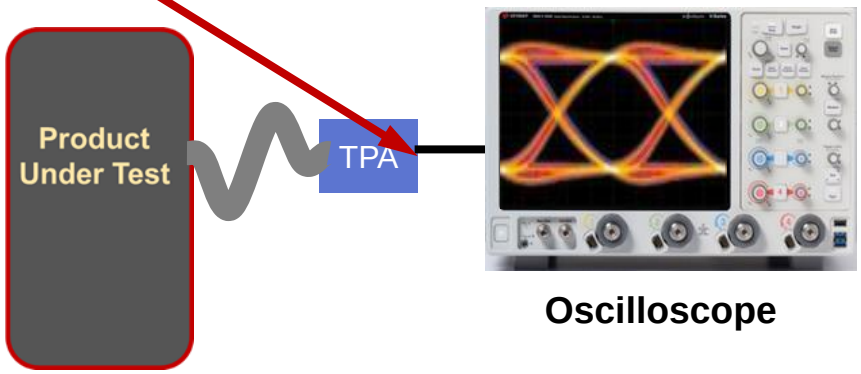


Transmitters are tested with testpoints TP2 or TP3Eq
Acquisition is at TP2 or TP3

TP2: fixture(TPA) is connected directly to device



TP3Eq:
TP2 acq with cable model + Eq Math, or,
TP3 acq + Eq Math



Physical Layer Testing: High speed data lanes

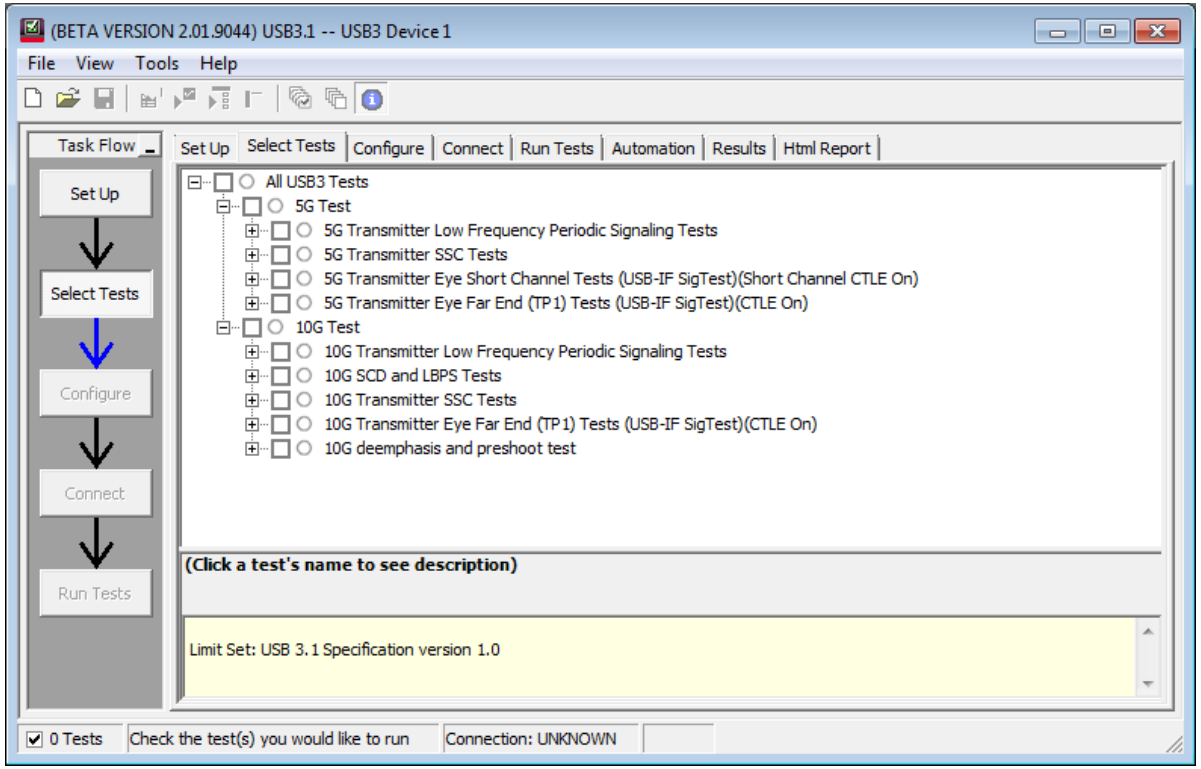
Transmitter Testpoints

Acquisition

Standard	TP2	TP3	TP3Eq	Comments
USB3.1compliance USB3.1 pre-comp	 x	x	Y Y	USB3.1 has various fixtures One connection testing. Test Mode signal compliance patterns
TBT3	x			PRBS31 is effectively random data signal.
DP1.4	x		Y	D10.2, PRBS7, HBR2CPAT
MHL3.3	x		Y	BIST randomized PRBS

Each Standard has its own suite of tests each with their own particular measurement processes.

Tx: Compliance Test Overview: USB 3.1, MHL, DP, TB



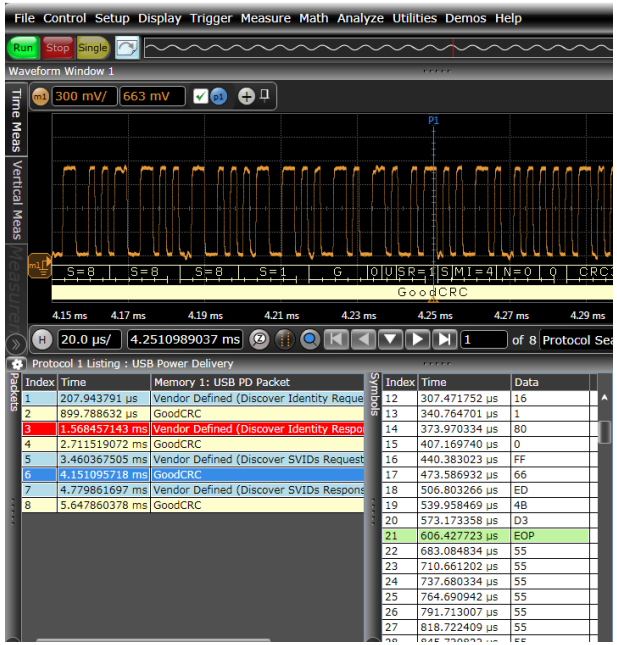
- Multiple Compliance Applications Releasing into the Type-C Eco-System
- USB 3.1 U7243B
- DP 1.3 U7232D
- Thunderbolt N6463B
- MHL 3.3 N6460B
- USB PD N8840A

An Entire Eco-System Enabled

Tx: Compliance Test Overview: New High Speed Fixture

- Highest signal integrity Type-C test fixture
- Type-C plug interface fixture handling connector “flip”
- Compliance test capability for USB 3.1, DisplayPort 1.3, Thunderbolt 2/3, MHL
- Best signal integrity: 20 GHz bandwidth (at -3 dB), de-embeddable up to 30 GHz
- Provides test point and probing access for transmitter and power delivery measurements
- Provides the elements to seamlessly leverage Keysight’s portfolio of compliance test applications

Tx: Special Decoders and Triggers for the Type-C Ecosystem



USB Power Delivery Decode

- Industry's only hardware based triggering
- Time aligned decoding
- Set up the entire trigger in 30 seconds
- Quickly scan through numerous events

USB 3.1 Decode

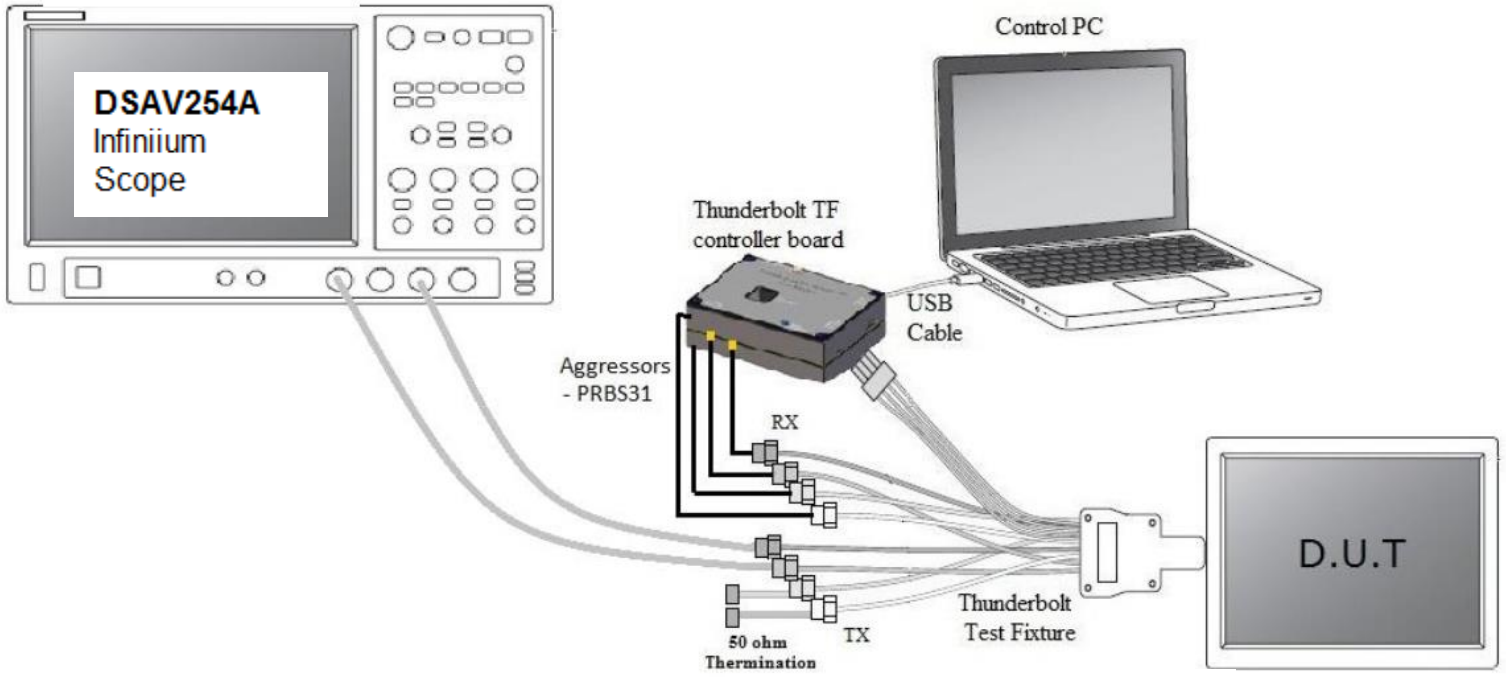
- Industry's only USB 3.1 decoder
- Time aligned decoding
- Quickly scan through numerous events

Physical Layer Testing: High speed data lane control

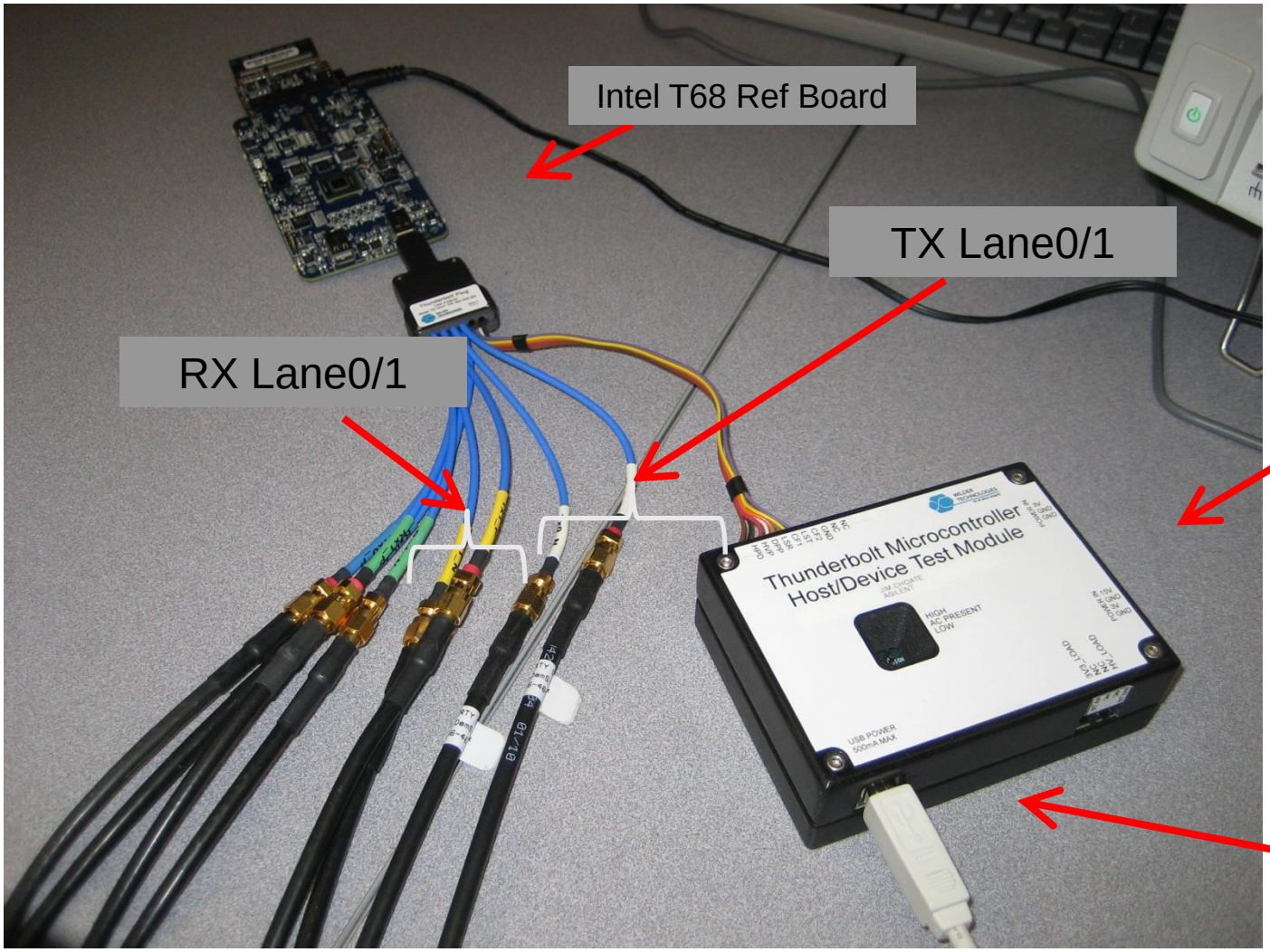
Standard/ Device	Needed for Control of device under test
All	Power Delivery Controller is required to set V_{Bus} setting, current or charge level if any, consumer or provider and to initiate alternate modes.
USB3.1TX	Compliance Mode by termination and LFPS ping, LBPM testing by LBPM initial simulation. HSETT for Hosts/Hubs
USB3.1 RX	Link Training Simulation through discovery and equalization processes to get into loopback.
TBT	TenLira SW from Intel to set up patterns and data rates
DP1.4 TX	Type C to DP adapter, DP Reference Sink, DPCD test modes active
DP1.4 RX	Type C to DP adapter, DP Reference Source, DPCD error counting active
MHL3.3	eCbus Controller and fixtures

Thunderbolt 3 Transmitter Test

- 25GHz BW required for compliance testing, more if closer to the silicon
- Thunderbolt-specific SW (Imaginarium, TenLira, TCL, scripts)
- Crosstalk generator
- Type-C test fixture
- UI, SSC, Rise/Fall, Jitter, Eye Diagram Near End/Far End
- New Preset testing and optimization for 10.3G and 20.6G



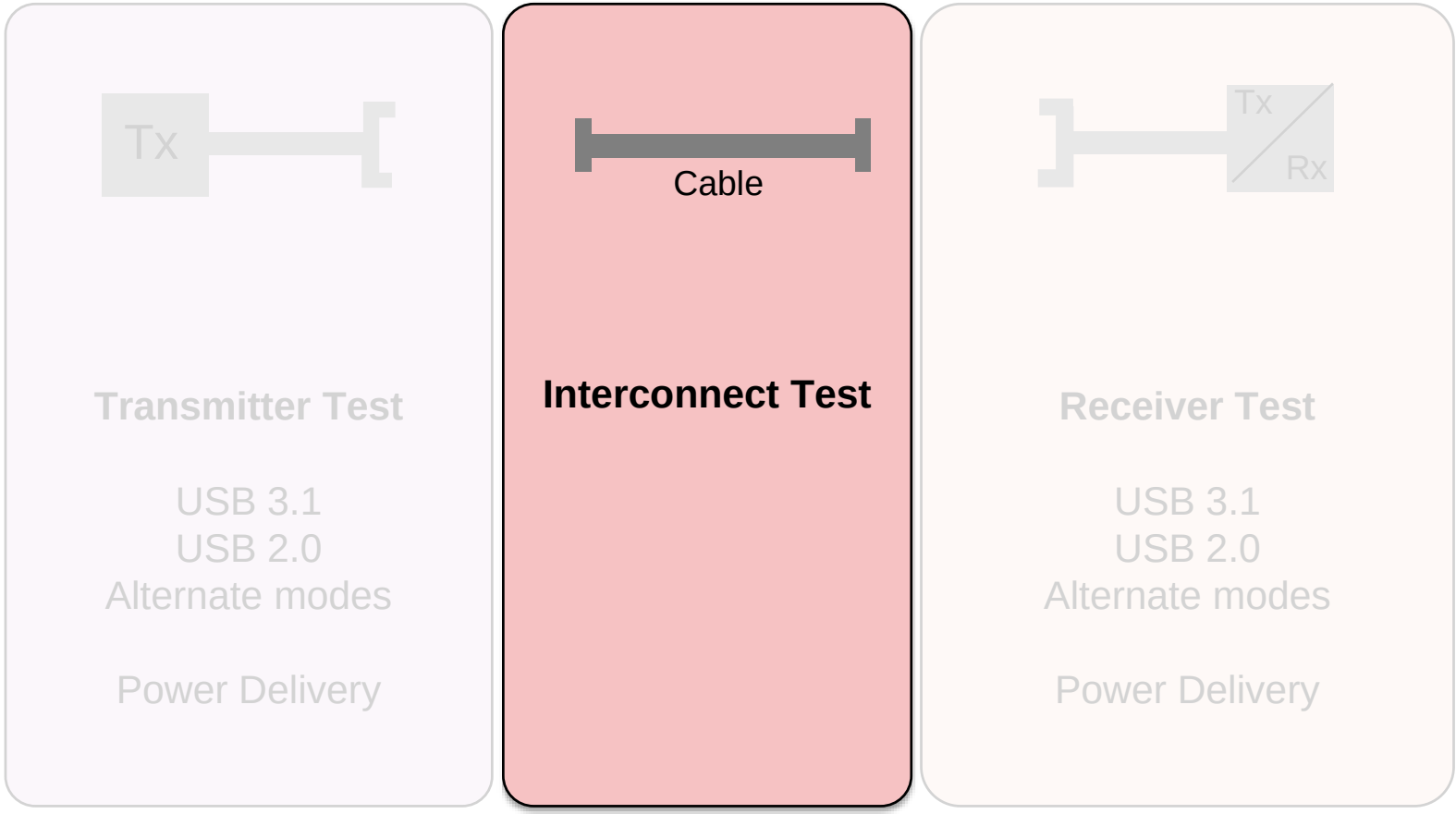
Thunderbolt TX and RX testing setup



TBT Microcontroller (put the device in test mode)

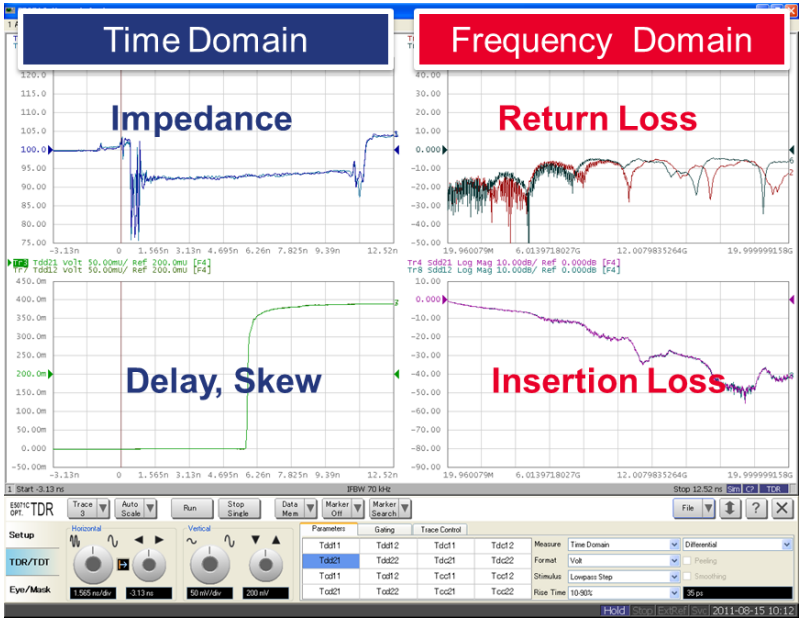
USB to Host SW

Type-C Design and Test Challenges: Overview

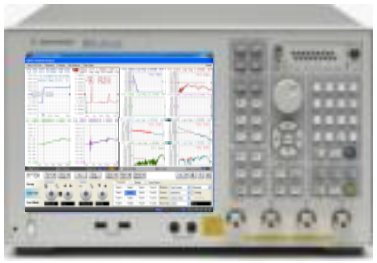


Type-C™ Cable/Connector Challenges

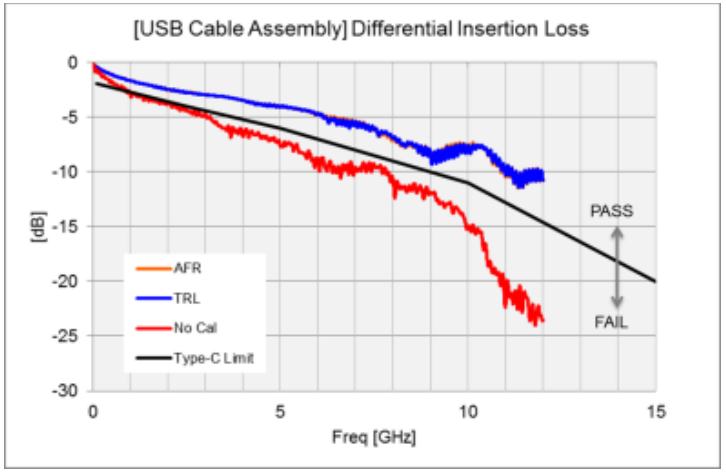
- Significant loss at higher frequencies require more rigorous approach to removing fixture effects, to measure the true performance of the device
- Channel response affected by many features in channel (loss, reflection, crosstalk, mode conversion)
- Managing EMI and RFI levels from the cable assembly

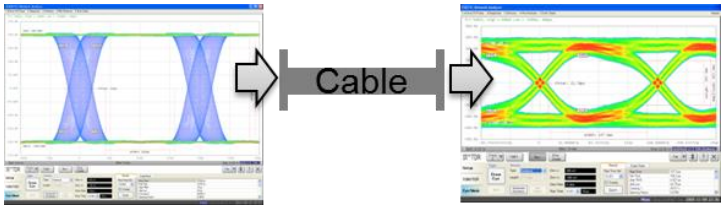


Type-C™ Cable/Connector Challenges



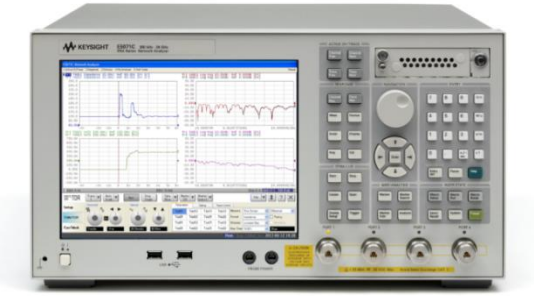
ENA-TDR Enhanced Time Domain Analysis Option with ECal Module (N4433A)





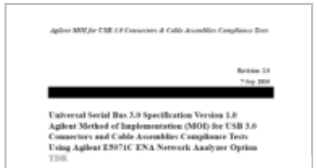
- Significant loss at higher frequencies require more rigorous approach to removing fixture effects
  - ➢ 2x thru de-embedding, or TRL calibration
- Channel response affected by many features in channel (loss, reflection, crosstalk, mode conversion)
  - ➢ Paradigm shift from traditional parametric testing to stressed eye testing (Channel Metrics/Margin)
- Managing EMI and RFI levels from the cable assembly
  - ➢ Cable Shielding Effectiveness

Type-C™ Cable/Connector Challenges



- ENA Mainframe
  - E5071C-4D5: 4-port, 300 kHz to 14 GHz
  - E5071C-4K5: 4-port, 300 kHz to 20 GHz
- Enhanced Time Domain Analysis Option (E5071C-TDR)
- ECal Module (N4433A)

(*) The list above includes the major equipment required. Please contact our local sales representative for configuration details.



MOI
(Method of Implementation)
Step-by-step procedure on how to measure the specified parameters in the specification document using ENA Option TDR.

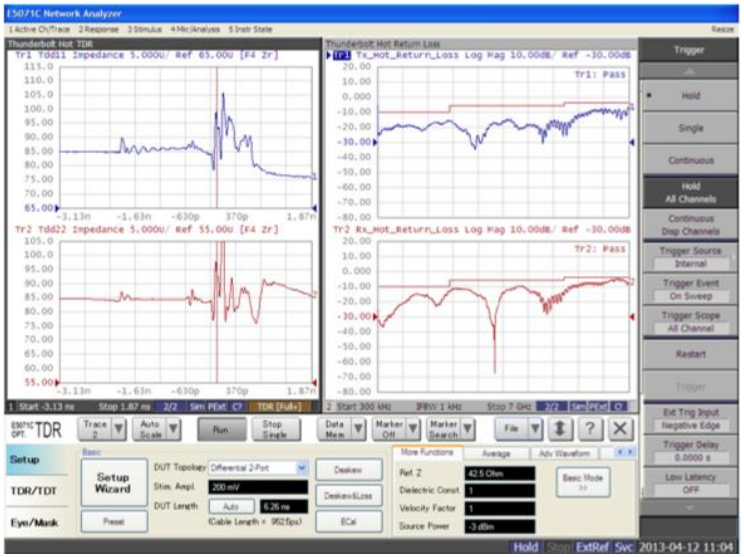
- Method of Implementation (MOI) document and instrument setup file will be made available for download on Keysight.com

Test Fixtures
Fixtures are available for purchase through Luxshare-ICT.
http://web.luxshare-ict.com/en/

ENA Option TDR is a authorized test tool for Cable PHY.
http://www.vesa.org/displayport-developer/certified-components/

Type-C™ Cable/Connector Challenges

– DUT output PRBS31 on all lanes with SSC turned on
– Setup the Network Analyzer with automated measurements specific to Thunderbolt 3



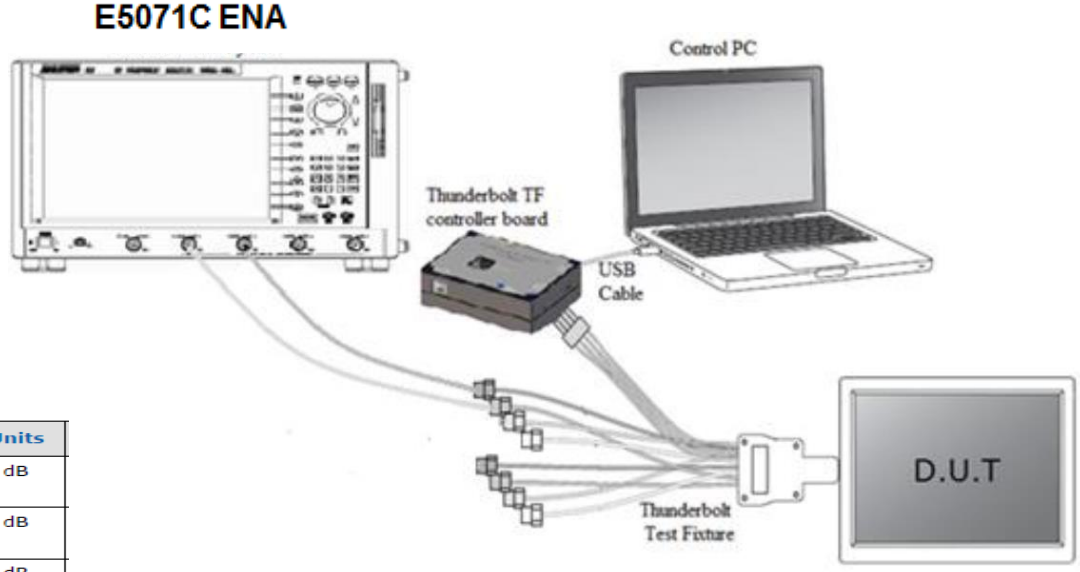


Table 4-6. Host/Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units
RL_LF	Return loss, 0.05 – 2 GHz	10		dB
RL_MF	Return loss, 2 – 5.2 GHz	6		dB
RL_HF	Return loss, 5.2 – 7 GHz	4		dB

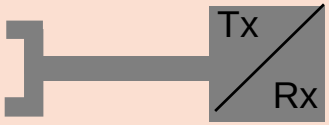
Type-C Design and Test Challenges: Overview

Transmitter Test

USB 3.1
USB 2.0
Alternate modes

Power Delivery

Interconnect Test



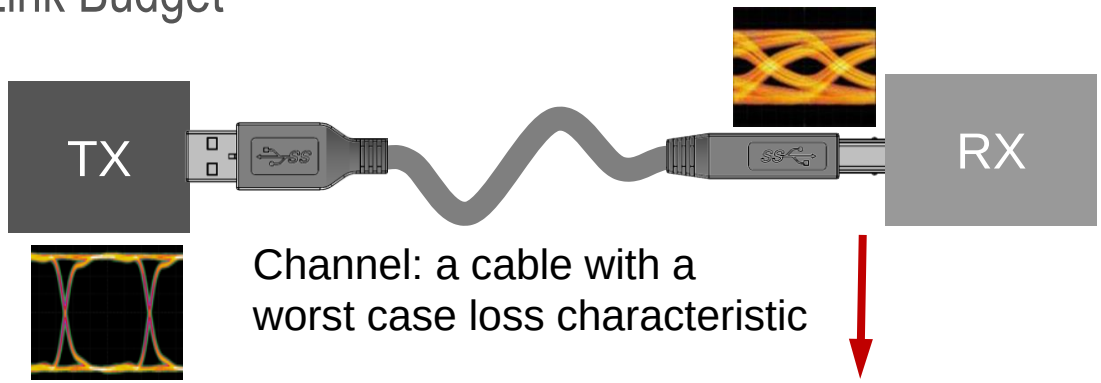
Receiver Test

USB 3.1
USB 2.0
Alternate modes

Power Delivery

Receiver Testing: High speed data lanes

Review: Link Budget



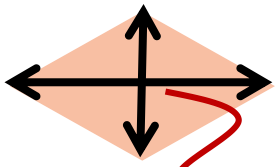
Channel: a cable with a worst case loss characteristic

- ✓ Minimum Amplitude
- ✓ RX Equalization
- ✓ Jitter tolerance
- ✓ Crosstalk

TX: Minimum Signal Fidelity

- ✓ Minimum and maximum amplitude
- ✓ TX Pre-Emphasis/Equalization
- ✓ TX Jitter
- ✓ Amplitude noise
- ✓ Transition time/BW

RX: Minimum Eye In (the impaired eye)

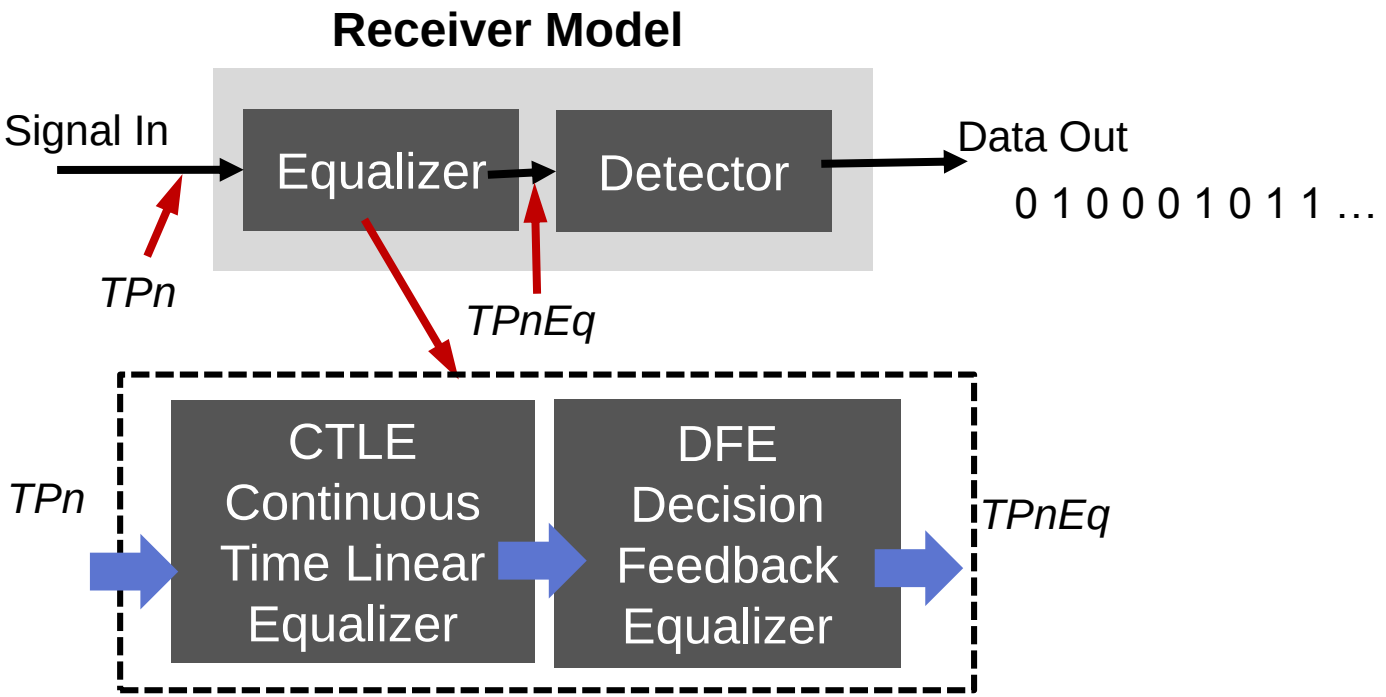


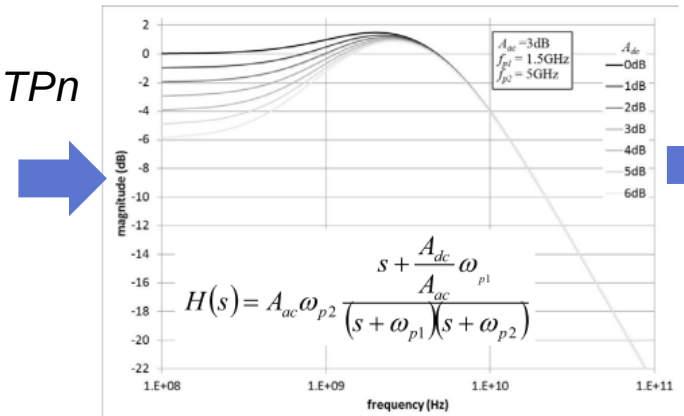
Receiver Detector

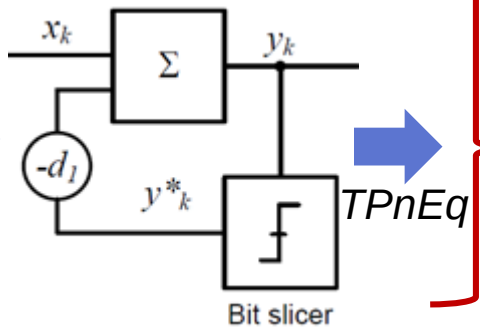
BER Out

A link with:
-a transmitter with minimum signal fidelity performance with,
-a cable that exhibits worst case characteristic (or better) and,
-a receiver that passes minimum eye requirement,
-> is guaranteed to work!

Receiver Testing: High speed data lanes

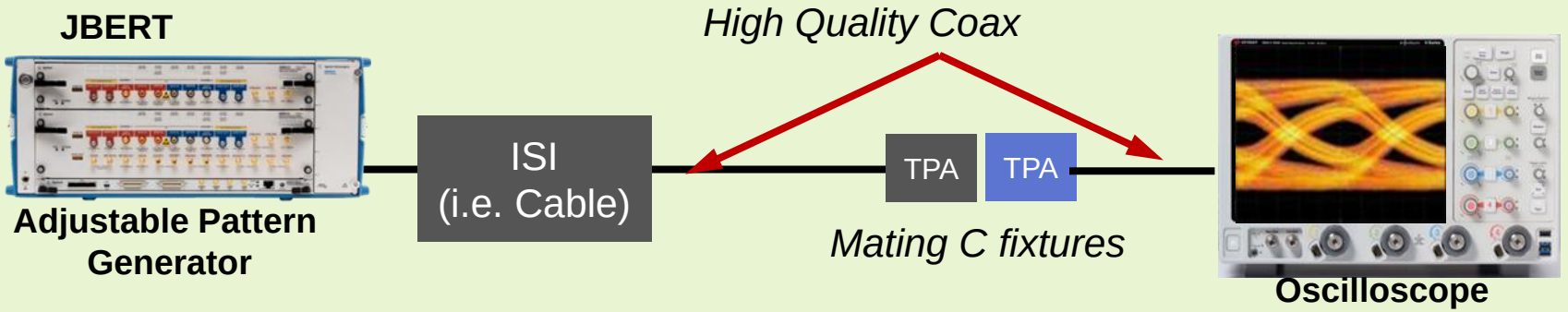




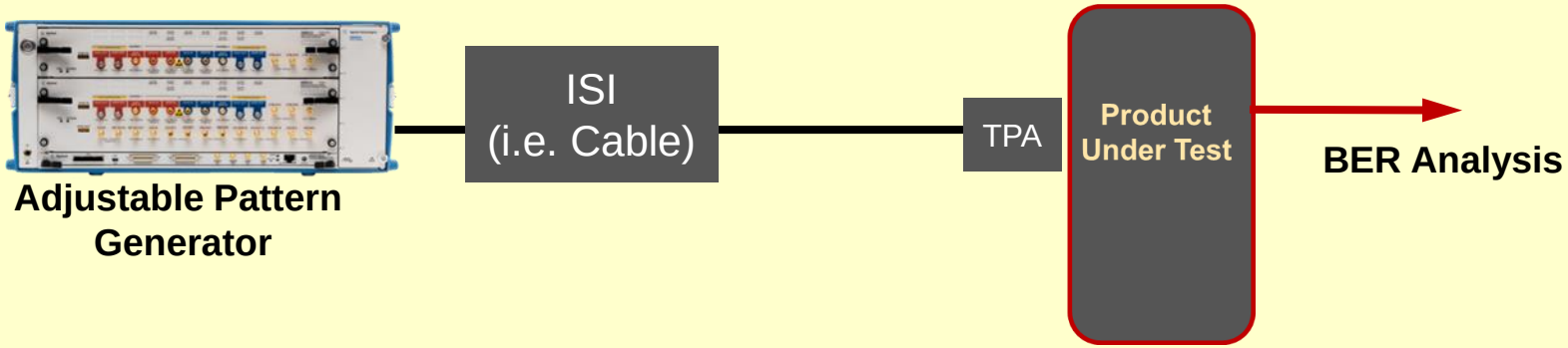


The CTLE and the DFE are mathematically implemented on an oscilloscope

Receiver Testing: High speed data lanes



Calibration: acquisition and mathematical processing for Equalization and Eye measurement to meet impaired eye requirement.



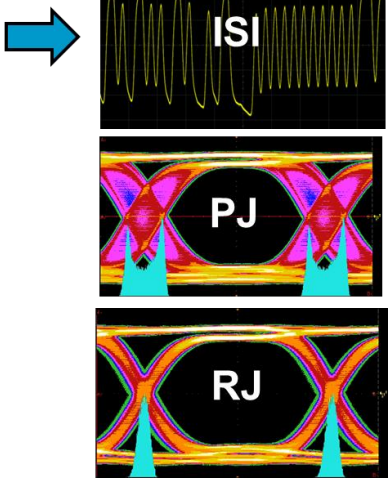
Test: Apply impaired signal, measure BER

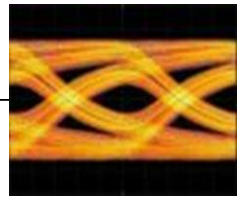
BER testing by:
-Loop back and BERT measurement.
-DUT Internal mode reporting BER

Receiver Testing: High speed data lanes

Standard	CTLE	DFE	BER Method	Comments
USB3.1	x	x	Loopback	Requires sophisticated protocol aware pattern generator to go through the link training process
TBT3			Internal	PRBS31
DP1.4	x	x	Internal	HBR2CPAT (2520 bit pattern)
MHL3.3	x		Internal	BIST randomized PRBS

Each Standard has its own ‘cocktail’ of jitter components and level settings to create the impaired eye. These components of jitter are measured by oscilloscope during calibration process.





M8020A JBERT

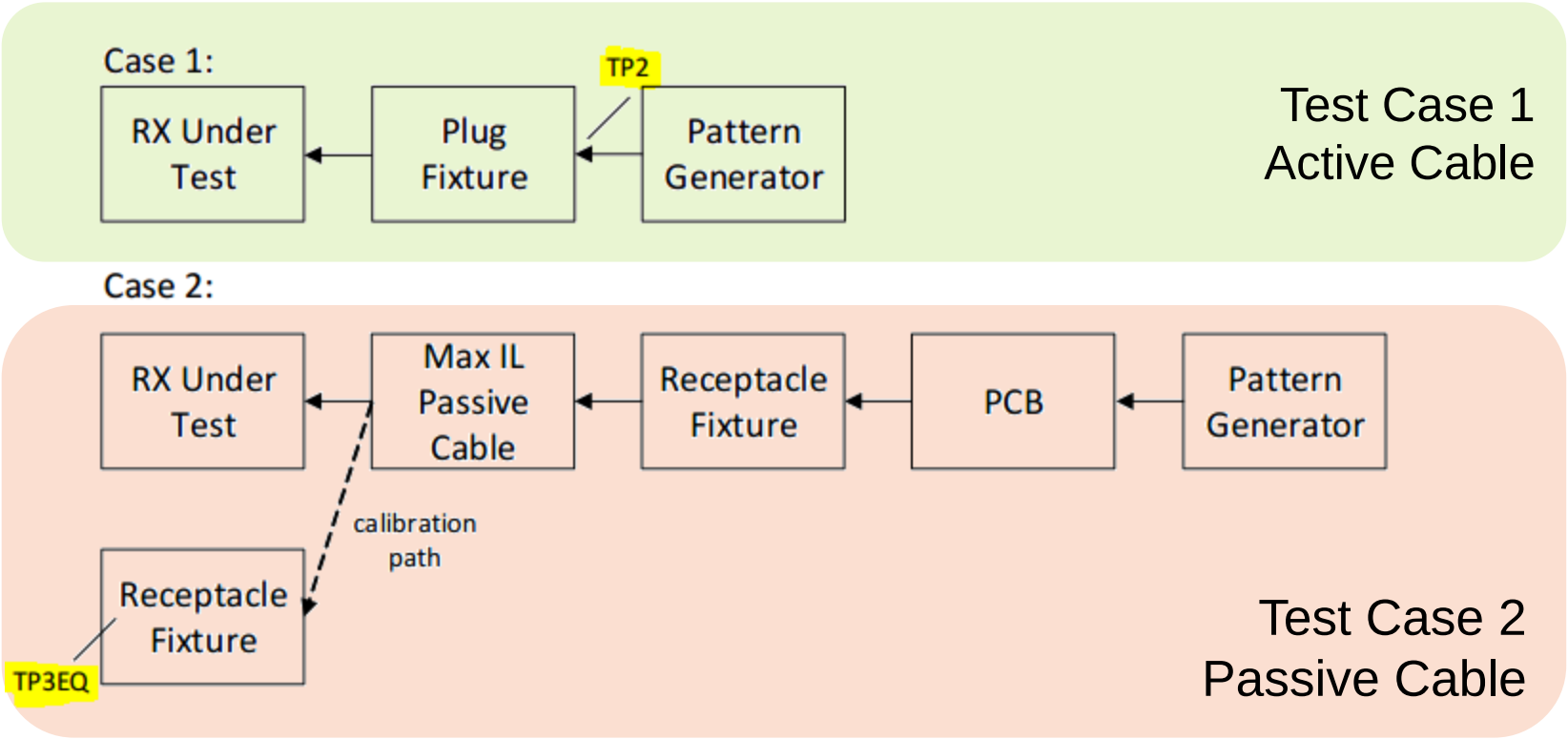
Thunderbolt - Jitter Impairment Calibration for RX testing

Host / Device 10G & 20G				
	Inner eye Voltage	Random Jitter	Periodic Jitter	Total Jitter
Test Case	(mV peak)	(UI pp)	(UI pp)	(UI pp)
1	350	0.14	0.17	0.38
2	35	0.14	0.17	0.66

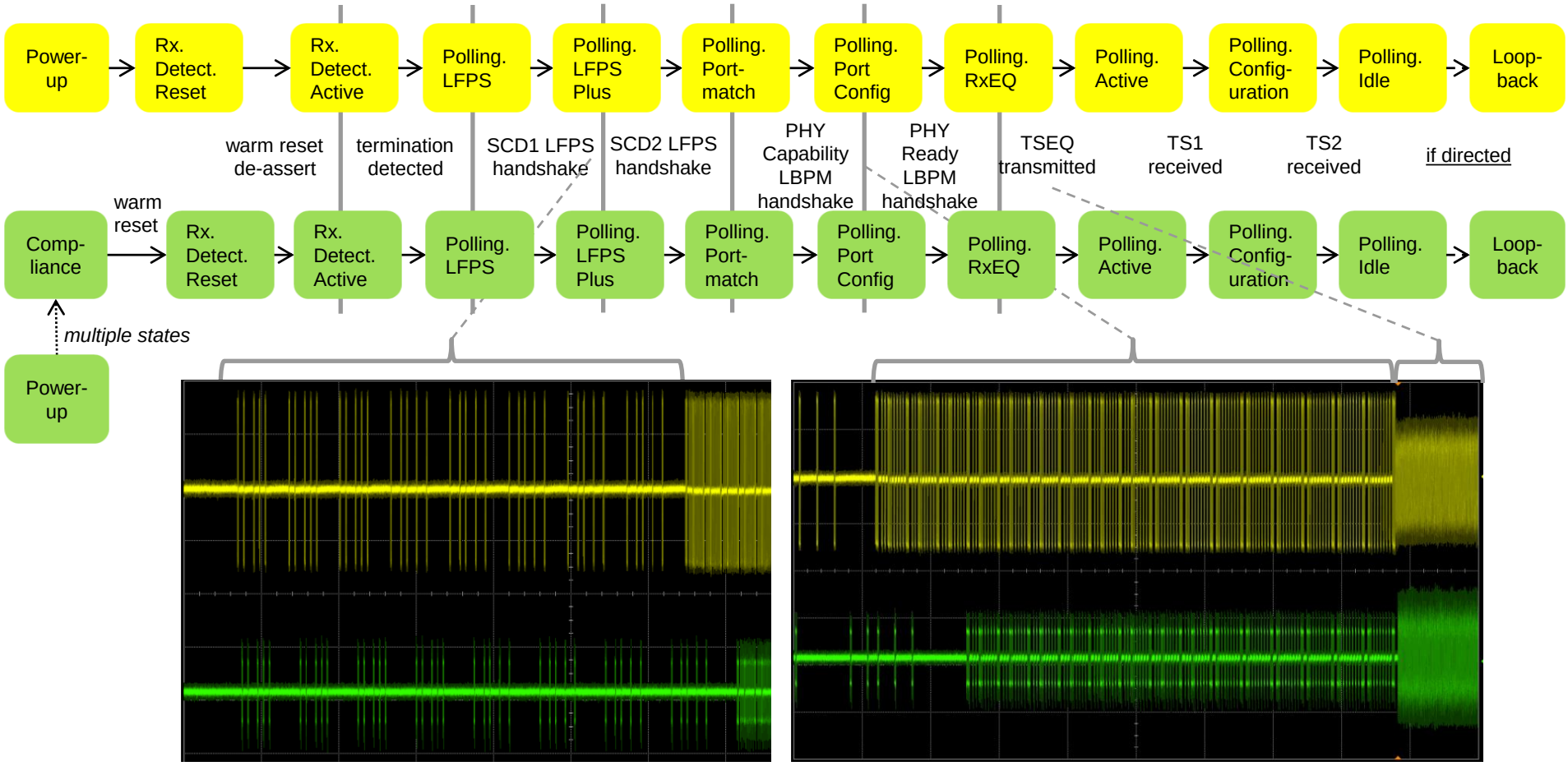
Note:

1. The device should be tested by injecting several different periodic jitter components, one at a time. The test should include at least the following **sinusoidal jitter frequencies: 1MHz, 2 MHz, 10 MHz, 50MHz, and 100MHz.**
2. AC common-mode noise should be added at the pattern-generator for ensuring worst-case transmitter characteristics. The total common-mode noise should be 100mV peak-to-peak, where the added noise profile shall be sine-wave at frequency not smaller than 400MHz.

Thunderbolt – Test Cases and Calibration Points

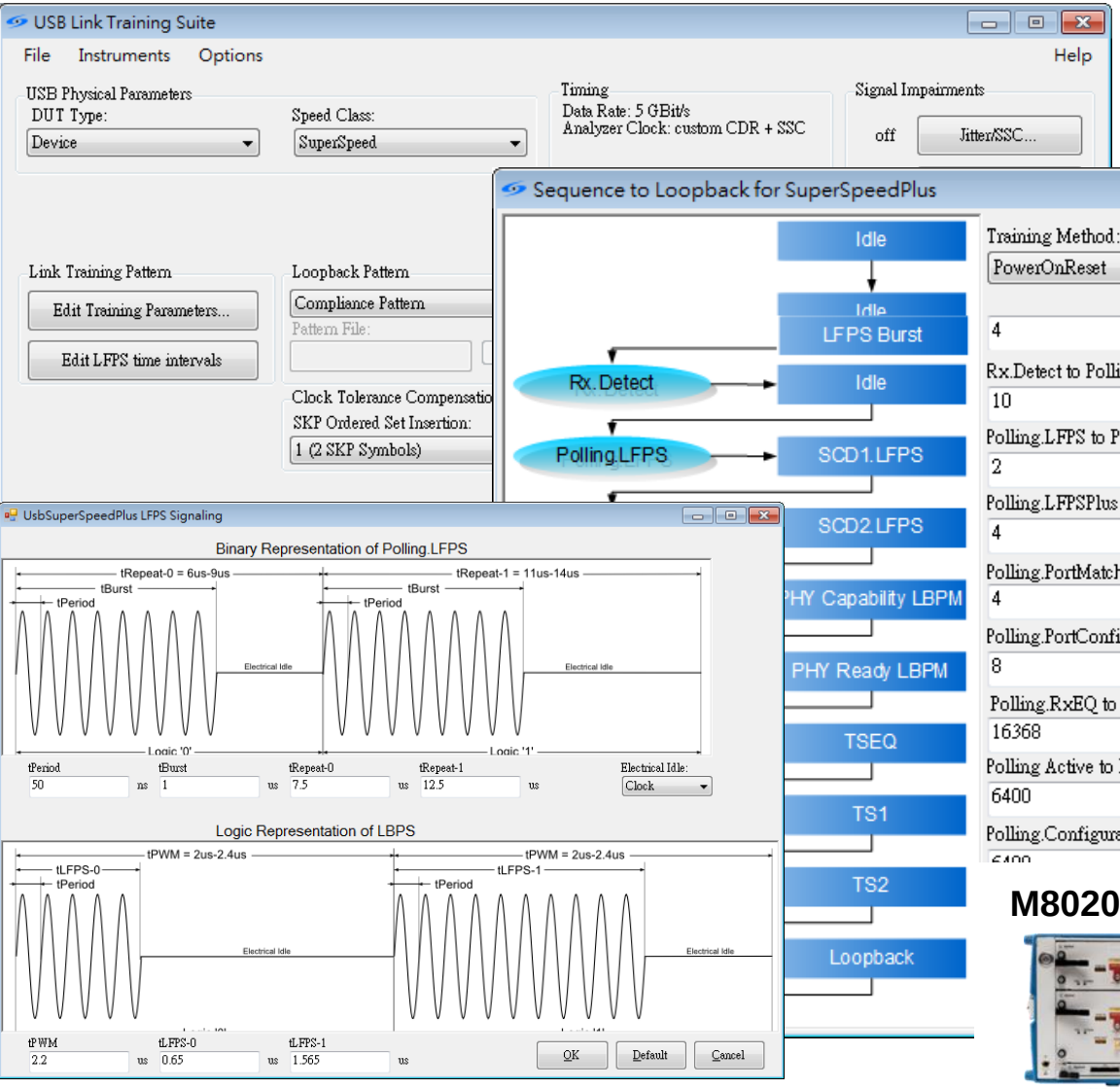


Receiver Testing: USB RX Test-Loopback



The DUT must brought through the whole link training state machine in order to get to the loopback state.

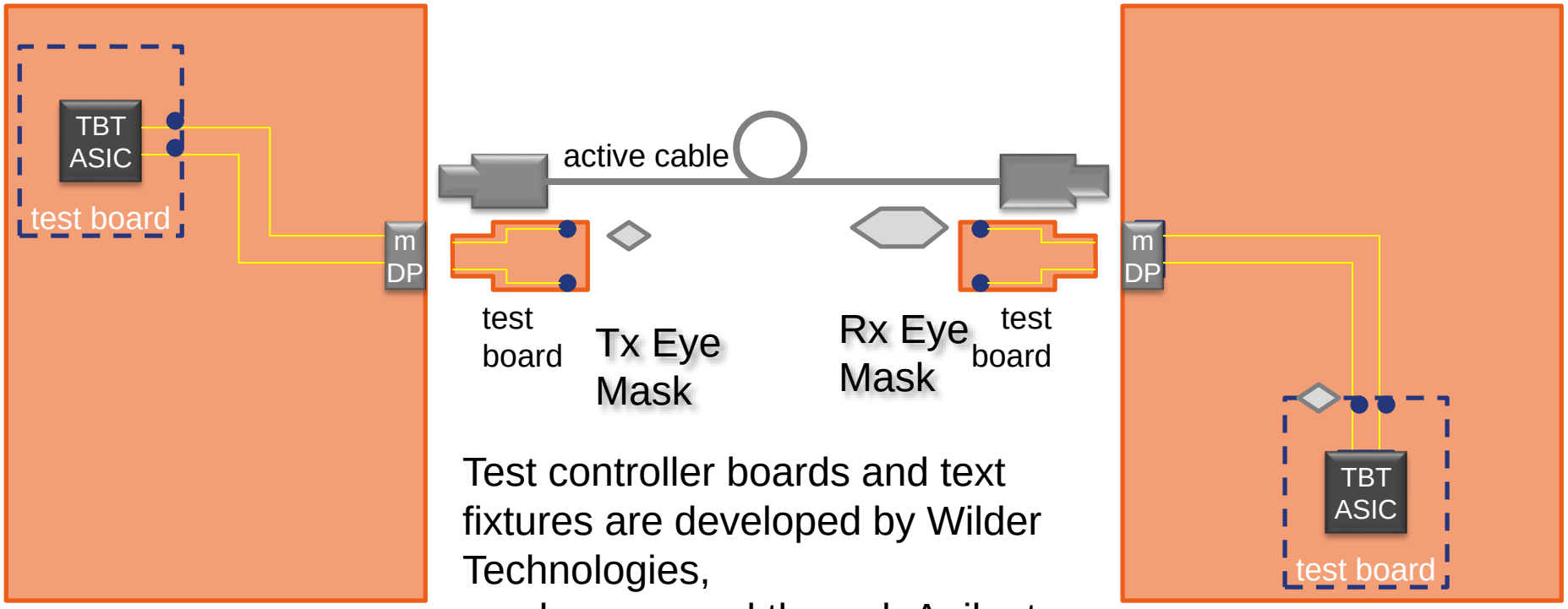
Receiver Testing: USB3.1 Loopback Training tool



M8020A JBERT

- USB Link Training Suite is a trainings sequence generation tool for USB3.1 Gen1/2
- Easy manipulation of
  - SCD1/SCD2/LBPM cycles
  - TSEQ count
  - TS1 count
  - TS2 count
- LFPS parameters adjustment:
  - tPeriod, tBurst, tRepeat, tPWM….
- Choice of:
  - Power On sequence
  - Warm Reset sequence

Thunderbolt System and testpoints



Test controller boards and text fixtures are developed by Wilder Technologies,
can be procured through Agilent

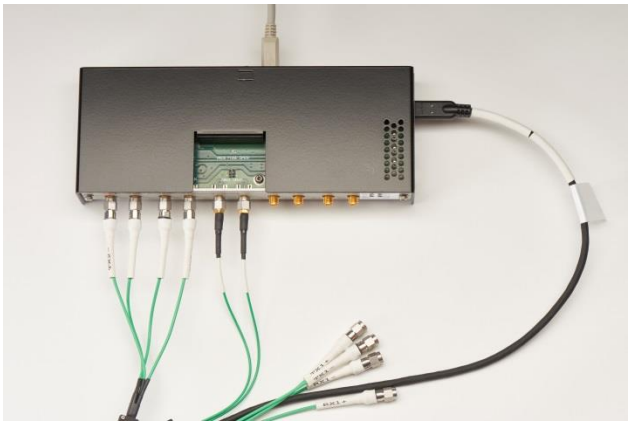
The active cable provides a very robust channel which doesn't need any kind of link training (unlike PCIe 3 for example). Therefore Rx and Tx physical layer compliance test is rather simple and straight forward.

Agenda

- Thunderbolt 3 Overview
- Measurement Challenges
- Tx Testing Solution
- Return Loss Testing
- Power Delivery Testing
- Rx Testing Solution
- Summary

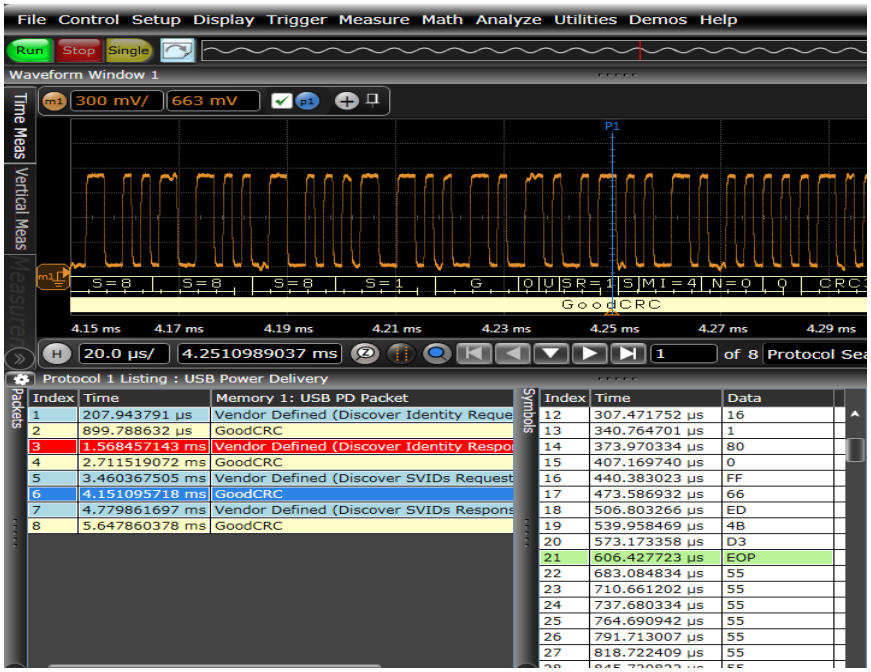
N7016A Type-C low speed signal access and control fixture

- Access to CC_1, CC_2, SBU1, SBU2, V_{BUS} and GND
- Controls to terminate CC1, CC2 independently (R_A, R_P, R_D)
- Control to load V_{CONN}
- External power for power consumers
- Type C receptacle to plug into other devices or cables (Port 2)
- USB2.0 interface for external control from application or standalone SW on a PC



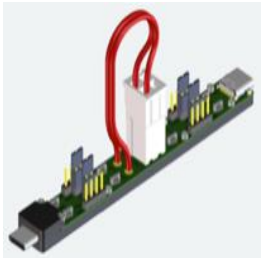
N8837A USB-PD Protocol Trigger and Decode

- Support for the USB-PD CC 4b/5b BMC encoded protocol.
- On-screen serial decode synchronized with the serial waveform
- 4b, 5b or Label display formats
- Unique listing-window view of data transfer information with an automatic click and zoom and column sort.
- Serial packet search with navigation controls
- Software trigger on search for orders Sets, Control Packets, Data Packets, and Errors.



Power Delivery: Physical Layer Compliance Test

- Keysight Infiniium S-Series Oscilloscope
  - N2873A Standard Passive Probes for CC and VBUS
- 1147B Current Probe for Load Current
- GRL-USB-PD Power Delivery SW
- USB-PD Coupon(s) from Wilder-Tech or Luxshare-ICT (USB3.1-C-PDC or TF21-215G USB-PD Coupon)
- GRL-USB-PD-C1 Controller
- Keysight Power Supply and Load

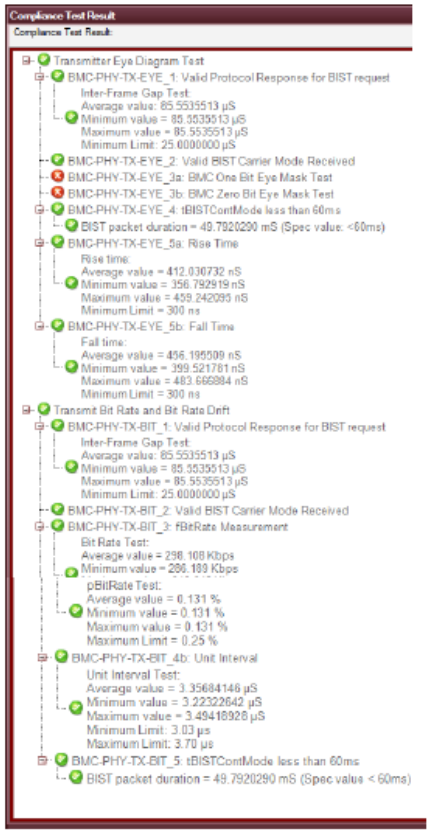


http://literature.cdn.keysight.com/litweb/pdf/5992-1463EN.pdf

Power Delivery: Physical Layer Compliance Test

Chapter 5

BMC PHY

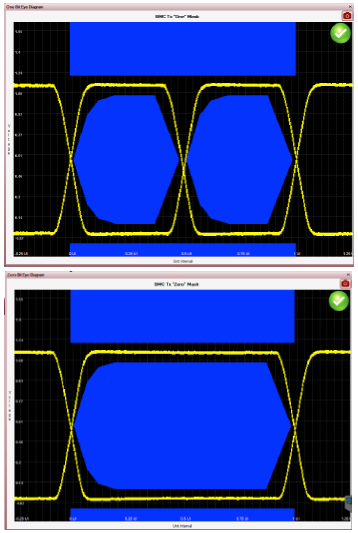


Power Loads and Transitions

- 12.11.1 POW_SRC_LOAD_P_PC
  - POW_SRC_LOAD_P_PC_1
    - DUT failed to send PING message when contracted to greater than 5V
  - POW_SRC_LOAD_P_PC_2
  - POW_SRC_LOAD_P_PC_PDO1_5V_3A
    - POW_SRC_LOAD_P_PC_3
    - POW_SRC_LOAD_P_PC_4
    - POW_SRC_LOAD_P_PC_5
    - POW_SRC_LOAD_P_PC_6
      - Load Current set to 0.75: Voltage drop = 0.032V (Limit: 0.25V)
      - Load Current set to 1.5: Voltage drop = 0.031V (Limit: 0.25V)
      - Load Current set to 2.25: Voltage drop = 0.265V (Limit: 0.25V)
      - Load Current set to 3: Voltage drop = 0.41V (Limit: 0.25V)
      - Load Current set to 2.25: Voltage drop = 0.283V (Limit: 0.25V)
      - Load Current set to 1.5: Voltage drop = 0.025V (Limit: 0.25V)
      - Load Current set to 0.75: Voltage drop = 0.044V (Limit: 0.25V)
  - POW_SRC_LOAD_P_PC_PDO2_12V_3A
    - POW_SRC_LOAD_P_PC_3
    - POW_SRC_LOAD_P_PC_4
    - POW_SRC_LOAD_P_PC_5
    - POW_SRC_LOAD_P_PC_6
      - Load Current set to 0.75: Voltage drop = 0.165V (Limit: 0.6V)
      - Load Current set to 1.5: Voltage drop = 0.075V (Limit: 0.6V)
      - Load Current set to 2.25: Voltage drop = 0.277V (Limit: 0.6V)
      - Load Current set to 3: Voltage drop = 0.422V (Limit: 1V)
      - Load Current set to 2.25: Voltage drop = 0.227V (Limit: 1V)
      - Load Current set to 1.5: Voltage drop = 0.007V (Limit: 1V)
      - Load Current set to 0.75: Voltage drop = 0.172V (Limit: 1V)
- 12.11.4 POW_SRC_TRANS_P_PC
  - POW_SRC_TRANS_P_PC_1
  - POW_SRC_TRANS_P_PC_2
    - POW_SRC_TRANS_P_PC_1_2
    - POW_SRC_TRANS_P_PC_2_1
    - POW_SRC_TRANS_P_PC_1_3
    - POW_SRC_TRANS_P_PC_3_2
    - POW_SRC_TRANS_P_PC_2_3
    - POW_SRC_TRANS_P_PC_3_1

Power Role Swap

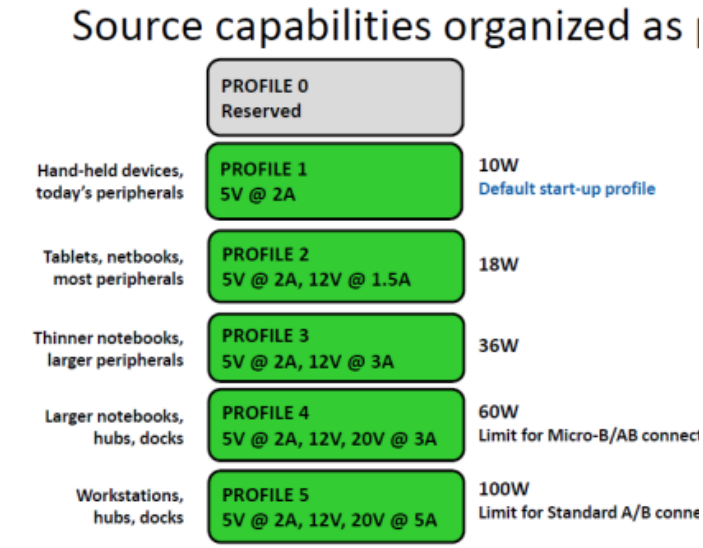
- POW_SWAP_PC_SRC_REQ
  - PROC_PD_MODE
  - PROT_PROC_SWAP_UUT_SRC
    - UUT could not initiate Power Role Swap
- POW_SWAP_PC_SNK_SRC
  - PROC-PD-MODE
  - PROT-PROC-SWAP-TSTR-SNK
  - PROT-PROC-SWAP-TSTR-SRC
- POW_SWAP_PC_SNK_SNK
  - PROC-PD-MODE
  - PROT-PROC-SWAP-TSTR-SNK
  - PROT-PROC-SWAP-UUT-SNK

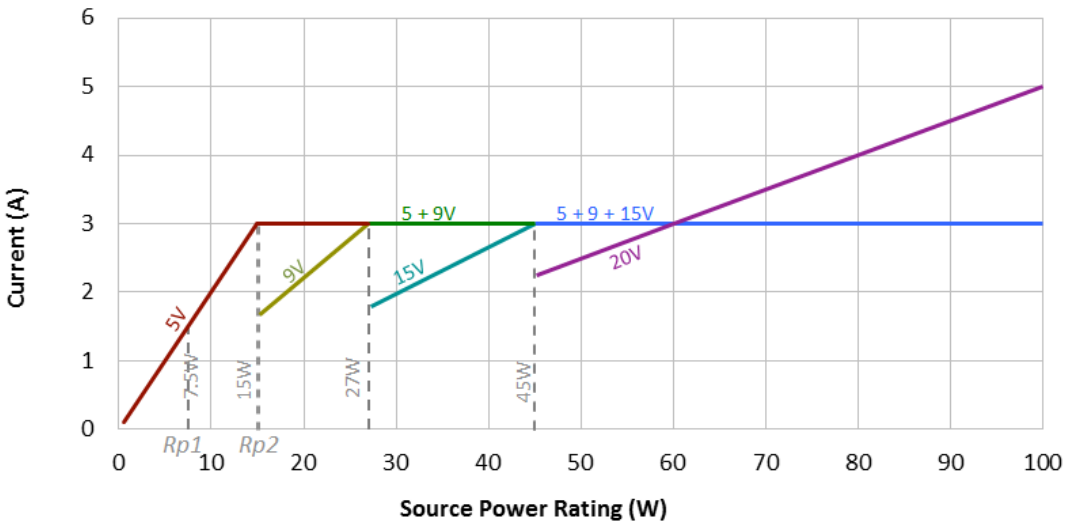


Power Delivery: Power Supply Profile Test

Chapter 7

- Chapter 7: Power Supply
  - Depending on Power Profile 1-5
  - Source or Load Requirements
  - Considering explicit Watts and Voltage





KEYSIGHT TECHNOLOGIES

Power Solutions for Type-C PD

Choose from these instruments that meet the requirements

N6700 series ***N6705B***

N6752A

N6705B DC Power Analyzer or N6700 Modular Power System with N6752A DC power module

Source: 50V, 10A, 100W

N3301A ***N3303A***

N3301A System DC Electronic Load with N3303A load module

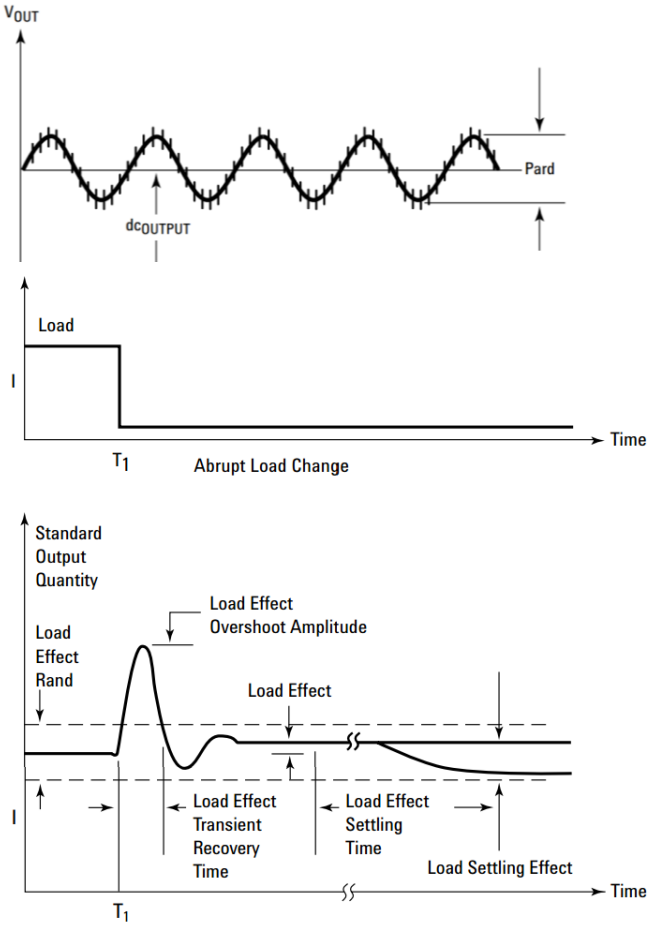
Load: 240V, 10A, 250W

– Sourcing and Loading
N6752A high performance DC source module and N3303A DC electronic load module meet stringent combination of requirements for slew rate, transient response and power demands of USB PD 2.0 validation testing

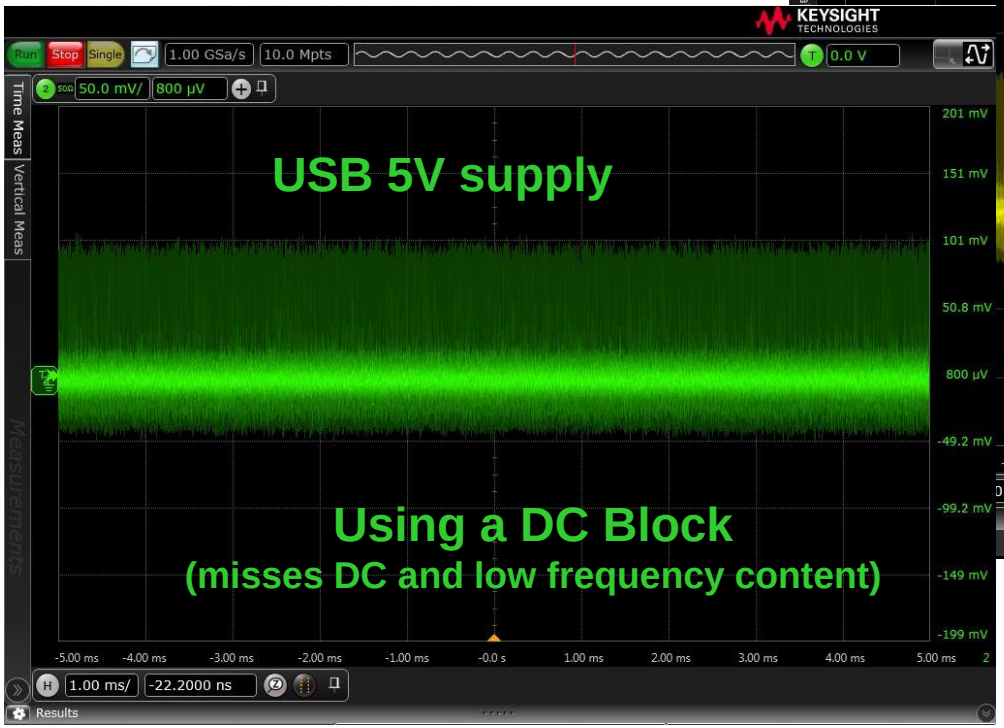
– Most ordinary power products do not meet the necessary combination of requirements

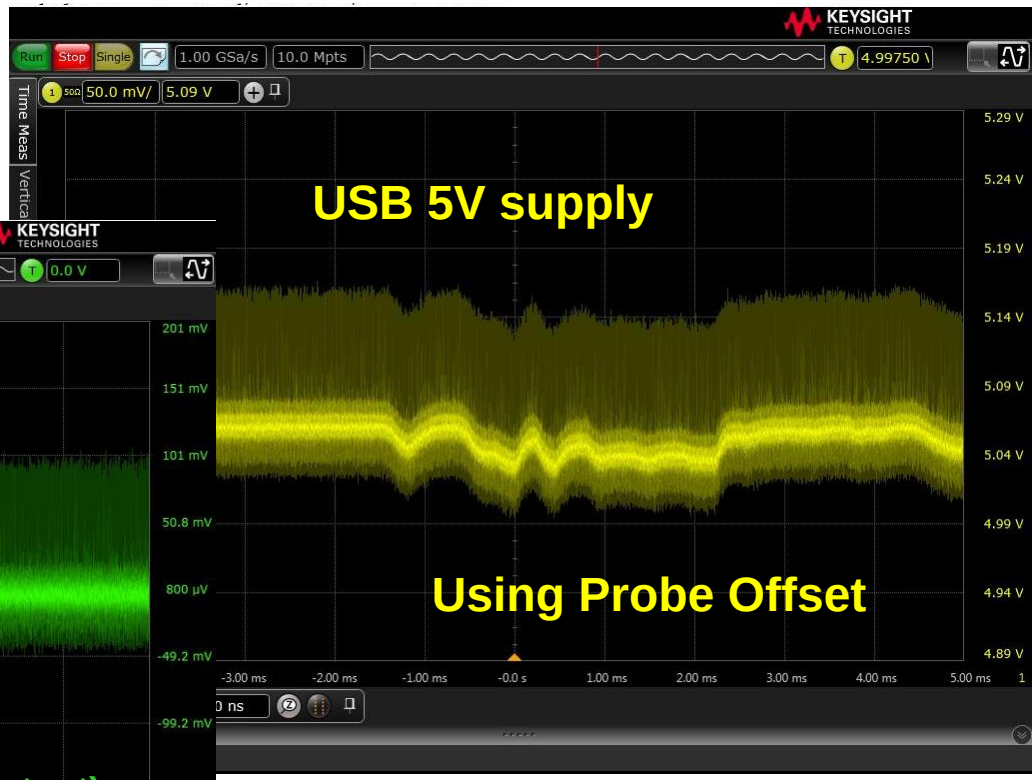
USB-PD Power Integrity Measurements

- Supply drift
- PARD (Periodic and Random Disturbances)—noise, ripple and switching transients on power rails.
- Static and dynamic load response.
- Programmable power rail response.
- High frequency transients and noise.
- Product electrical validation at extended temperatures.



Large DC Offset—Probe Offset or DC Block





DC Block

N7020A Power Rail Probe

Characteristics and Specifications: N7020A Power Rail Probe	
Probe Bandwidth (-3dB)	**2GHz**
Attenuation Ratio	**1:1**
Offset Range	**± 24V**
*** Input Impedance @ DC**	**50kΩ +/-2%**
Active Signal Range	± 850mV about offset voltage
Probe Noise	**10% increase to the noise of the connected oscilloscope**
Probe Type	Single-ended
Included accessories	N7021A—Coaxial Probe Head (qty 3) ($175 us)
	N7022A –Main Cable ($240)
Maximum non-destructive input voltage	+/-30V (DC + peak AC)
Output impedance	50Ω
Cable length	N7021A Main Cable: 48” N7022A Coaxial Probe Head: 8”
Ambient operating temperature	Probe Pod: 0 – 40°C, **N7021A main cable, N7022A coaxial probe head: 0 – 85° C**

N8833A Crosstalk Analysis Tool

– Helps in identifying, quantifying and removal of crosstalk for analysis.

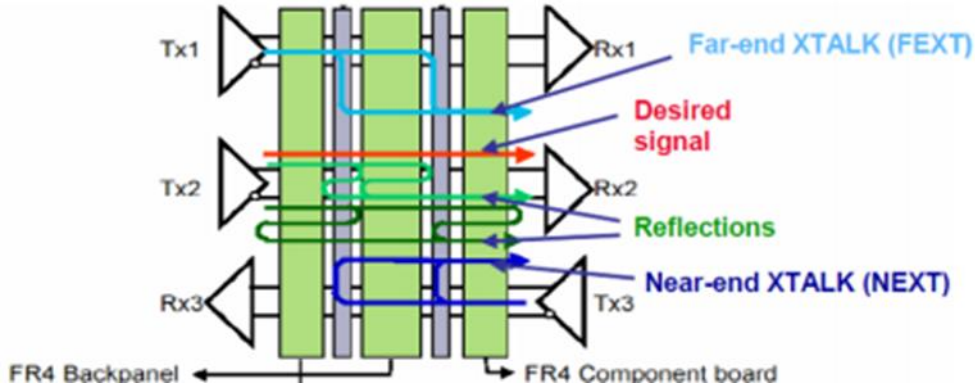
– Analyze up to four signals at once

– Identify the aggressor(s)

– Identify the victim

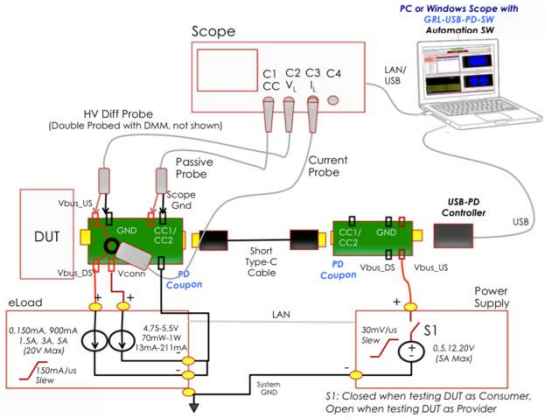
– NEXT and FEXT

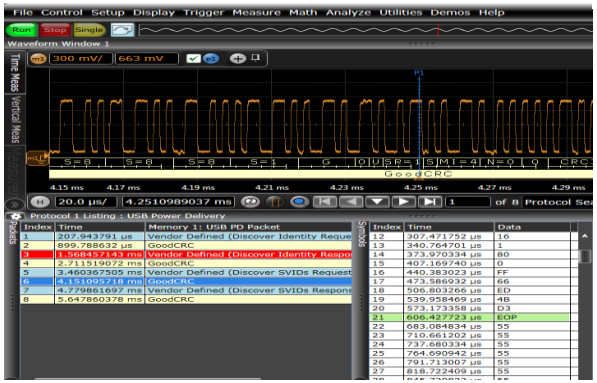
– Power supply analysis (aggressor and victim)

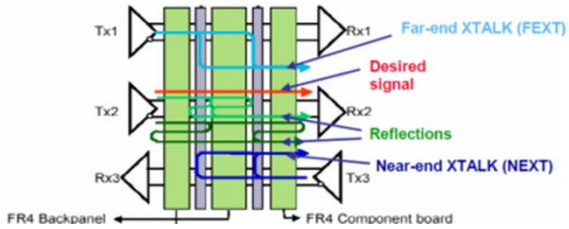


USB-PD Test Solutions Overview

- N7020A PD Probe
- N7016A PD Test Fixture
- N8837A PD Decode SW
- N8833A Crosstalk Analysis SW
- Portfolio of Power Sources and Loads
- GRL USB-PD PHY Compliance Solution







KEYSIGHT TECHNOLOGIES

Example Device

Your Type C device is USB3.1 Gen2 enabled and has a DP TX alt mode (4 lane) and will be a power provider at 18W profile

You will need to address:

Standard	Protocol	Phy Layer
USBPD2	X	X (PD Comm on cc1 and cc2, I and V for Vbus)
USB2.0	X	X (RX & TX)
USB3.1	X	X (HSD: RX & TX)
DP1.4	X	X (HSD: TX)/AUX Channel

Focus on the New

Product Under Test

Example Device: Getting Started

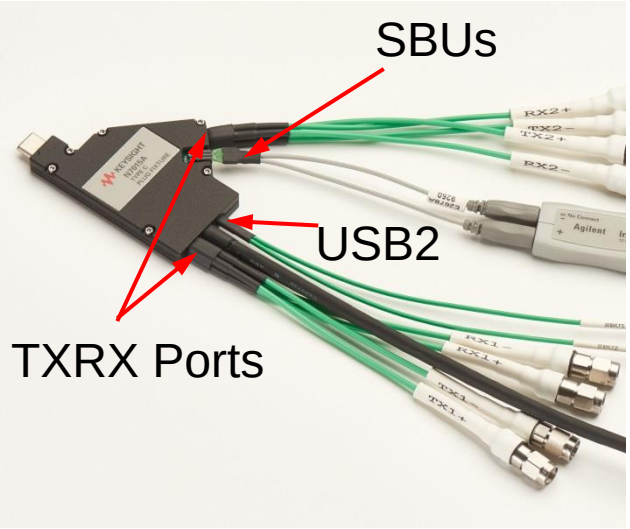
First step…..Signal Observation, Access and Control.

– Consider test fixtures N7015A, N7016 and the flexibility they bring.

– Phase matched cables. Adapters etc.

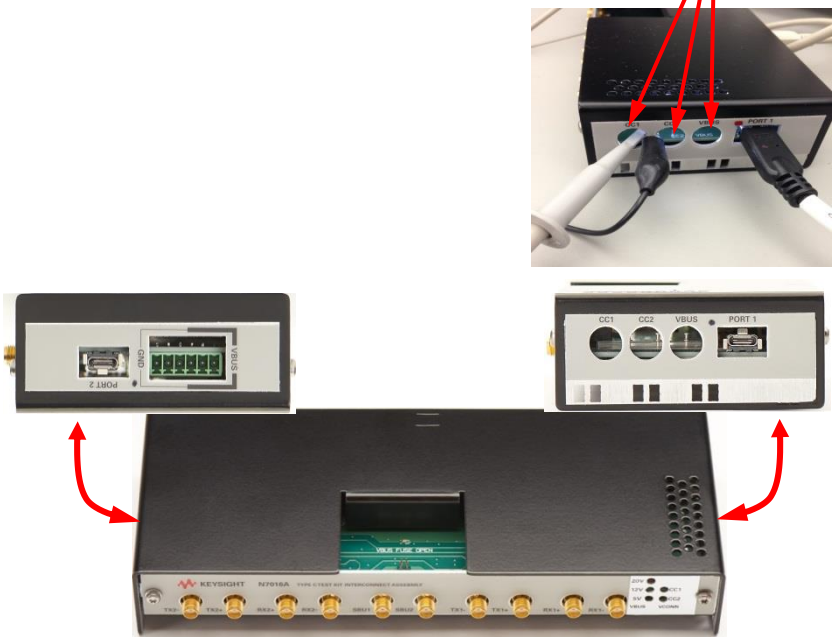
– Acquire various link partners

Product Under Test



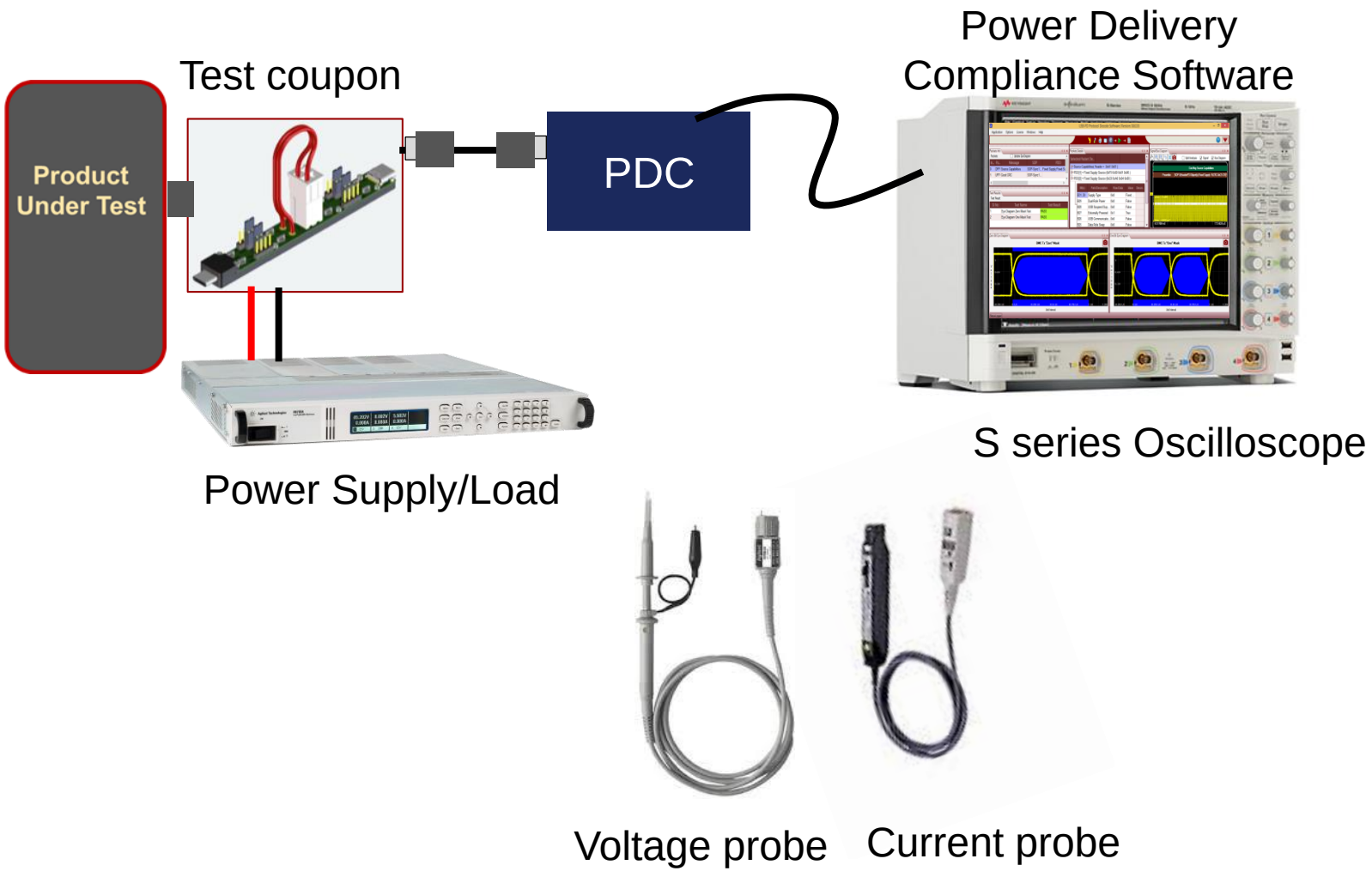
N7015A USB Type C
High Speed Fixture

CC1/2 V_{Bus}



N7016A USB Type C
Low Speed Fixture

Example Device: Power Delivery



Example Device: USB3.1 RX

Mating Fixture

Plug Fixture

RX
TX
RX
TX

Port 1
Port 2

ISI

CLE1000

V series Oscilloscope

Calibration Setup

Product Under Test

Plug Fixture

RX
TX
RX
TX

Port 1
Port 2

ISI

CLE1000

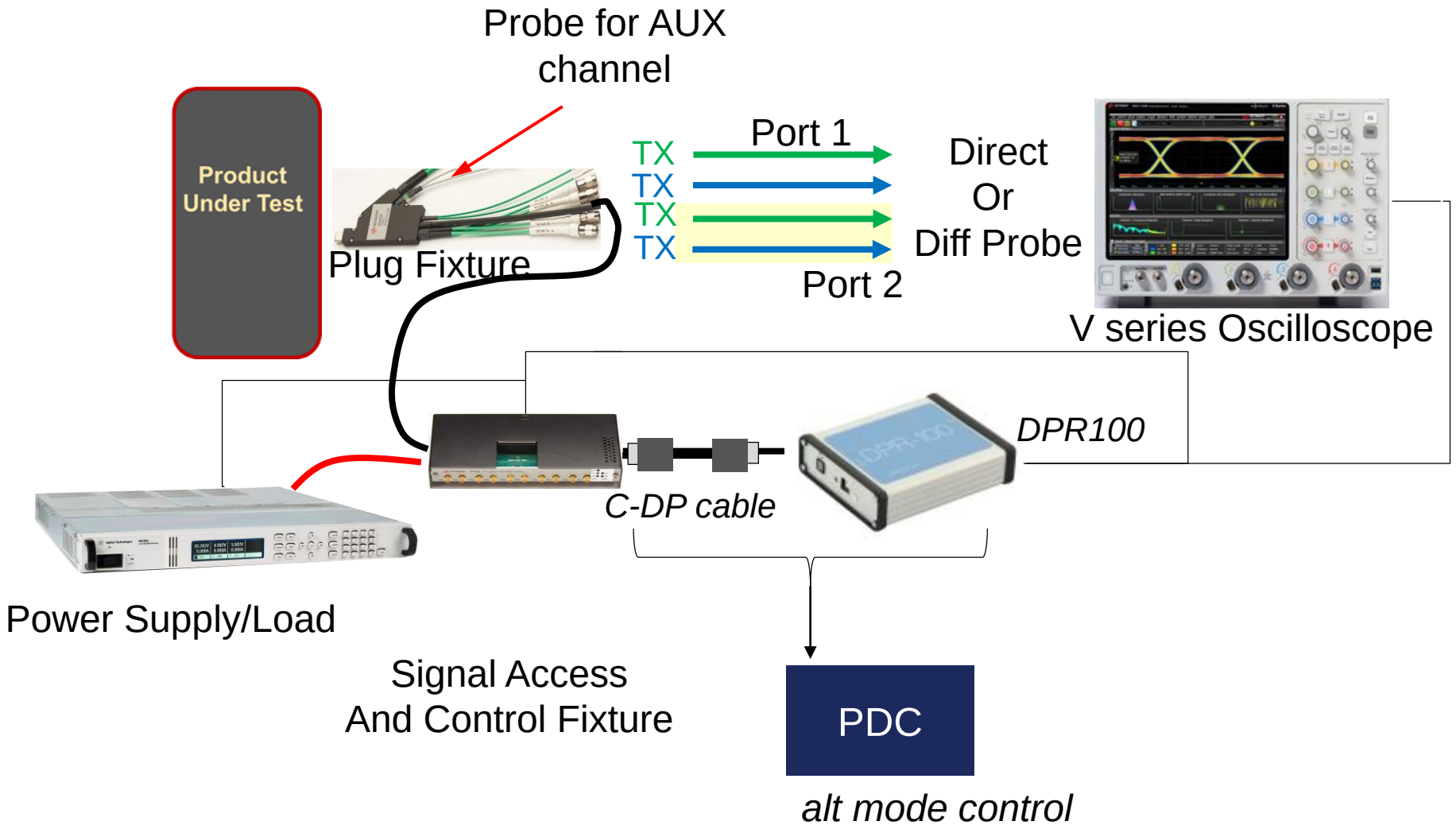
Signal Access and Control Fixture

PDC

Power Supply/Load

Test Setup

Example Device: DisplayPort TX



Keysight DisplayPort1.3 Solutions

Source Test Solution


Computer Motherboards, ICs, Graphic Cards

V-Series Infiniium Oscilloscopes

Unigraf DPR-100 For automation

U7232D DisplayPort Compliance Test SW

STD/mDP

Wilder TPA

USB C

N7015A TPA

Media Testing

Cables, PC Boards, Connectors

E5071C ENA

STD/mDP

BIT-DP-CBL-0002

USB C

Luxshare Rec

Sink Test Solution

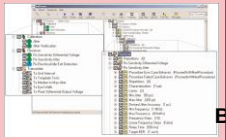
PC Monitors

Artek CLE1000

M8020A JBERT

N4915A-006 DP ISI Generation

Unigraf DPT-200 for Automation



N5990A Rx Compliance Test SW

STD/mDP

BIT-DP-RTF-0002

Wilder TPA

USB C

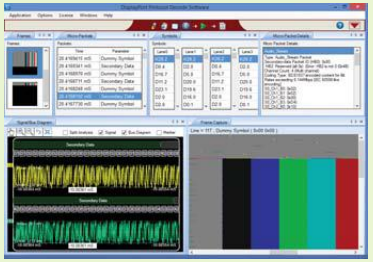
Luxshare Rec

N7015A TPA

Link Layer & General Solutions

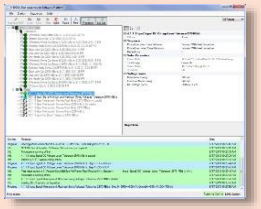
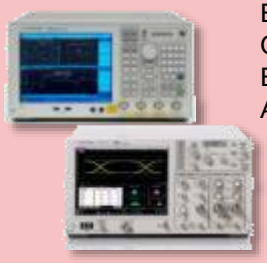
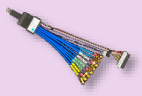
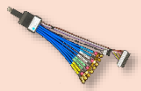
Protocol Debug solution

Granite River Labs GRL-DP-DEC




Main Link Analysis 16900A w/FS4430 From FuturePlus

Thunderbolt 3 – Total Solution

	Transmitter Test	Return Loss Test	Receiver Test
SW	 Thunderbolt Transmitter Test Software		 N5990A Automatic SW for TBT compliance
HW	TBT-TPA-UGH2 Controller   V-Series Infiniium Oscilloscope	 E5071C Option TDR ENA Network Analyzer or 86100D DCA-X	M8020A J-BERT High-Performance Serial BERT M8062A 32 Gb/s Multiplexer with De-emphasis  TBT-TPA-UGH2 Controller   81160A Common Mode Source
Fixture	 	 	 
DUT	Tx	Cable	Rx Error counter

Keysight USB 3.1/DP Test Solution

Design Simulation, USB-PD, and Channel Characterization

SW

HW

Fixture

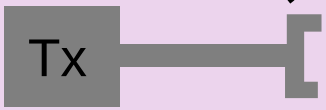
DUT

Transmitter Test

U7243B
USB Compliance Test Software

DSAV254A
Infiniium Scope

N7015A/16A
Tx Test Fixture

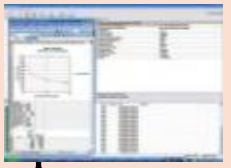


Interconnect Test

E5071C ENA Option TDR

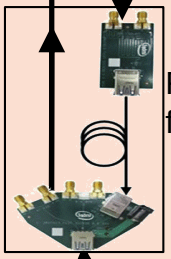
Cable/Connector Test Fixture

Receiver Test

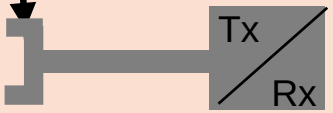


N5990A
USB Compliance Test Software

M8020A J-BERT High-Performance Serial BERT



Rx Test Fixture from USB-IF



Advantages of Keysight Solution

– Keysight is the only vendor approved for Tx, Rx as well as Return Loss Testing

– Compliance Test Specification conformant test setup, characterization and test

– Simple, repeatable automated and unattended calibration and test execution using automation SW for Tx and Rx Test

– All Type-C PHY standards are addressed by Keysight's Test platform

  • Thunderbolt

  • USB

  • DisplayPort

– Keysight can help with pre-compliance testing

Questions?

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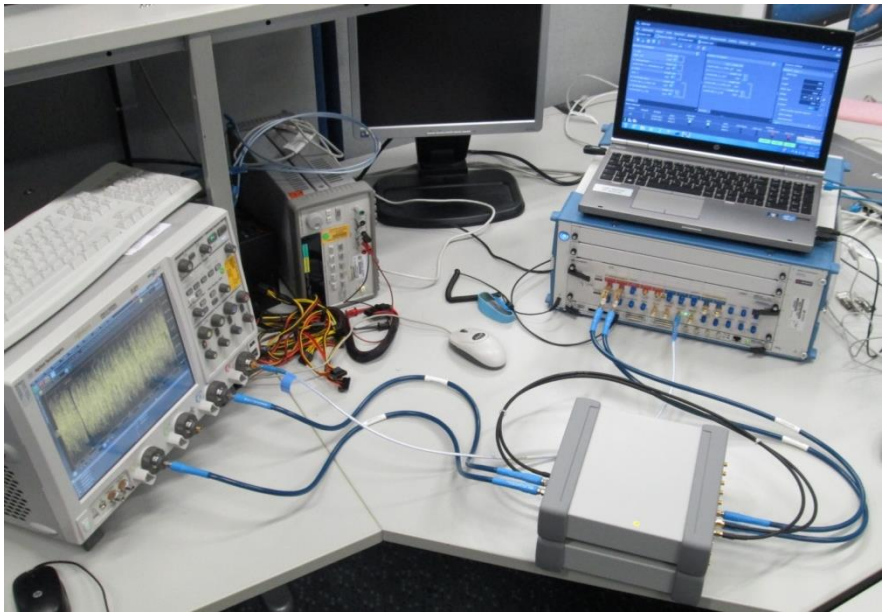
Engenheira de Aplicações
juliana.freire@keysight.com



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